Intel® 830M4 Development Platform

Schematic Diagrams

October 2004

Revision 1.1

Reference Number: **C87074-002**

Contents

Revision History

Date	Revision	Reference #	Description
August, 2004	1.0	C87074-001	Initial release of this document.
October, 2004	1.1	C87074-002	Updated Board revision. Added New Audio Chip STAC9766 - pg 28 of the schematics Fixed VCCP Load Line Fix audio GND connection; resistor R2D2 & R2E10, removed the Empty population - pg. 28 of the schematics Add a 1uF Capacitor and a 22-kohm resistor to the RTCRST# signal as RC delay circuit - pg. 18 of the schematics Changed R8J4 to 174 ohm, 1% to fix the load line issue - pg. 39 of the schematics

Introduction 1

This document provides schematic diagrams for the Intel® 830M4 Development Platform system components.

1.1 Intended Audience

The Schematic Diagrams are intended to provide detailed, technical information about the Intel® 830M4 Development Platform and its components to the system integrators, engineers and technicians who need this level of information. The Schematic Diagrams are not intended for general audiences outside the technical ranks mentioned above.

1.2 Schematics

Schematic diagrams are provided on the following pages.

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
-002	NEW AUDIO CHIP						
C	FIX VCCP LOAD LINE FIX AUDIO GND CONNECTION						
D	ADD CAP TO RTCRST CKT CHANGE LOAD LINE SETTING RESISTORS IN VCCP SUPPLY						

INTEL(R) 830M4

LV/ULV CELERON/830M/ICH4

FAB D
SCHEMATIC REV 1.00

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

SEE COVER SHEET FOR SCHEMATIC DOCUMENT NUMBER

DRAWING

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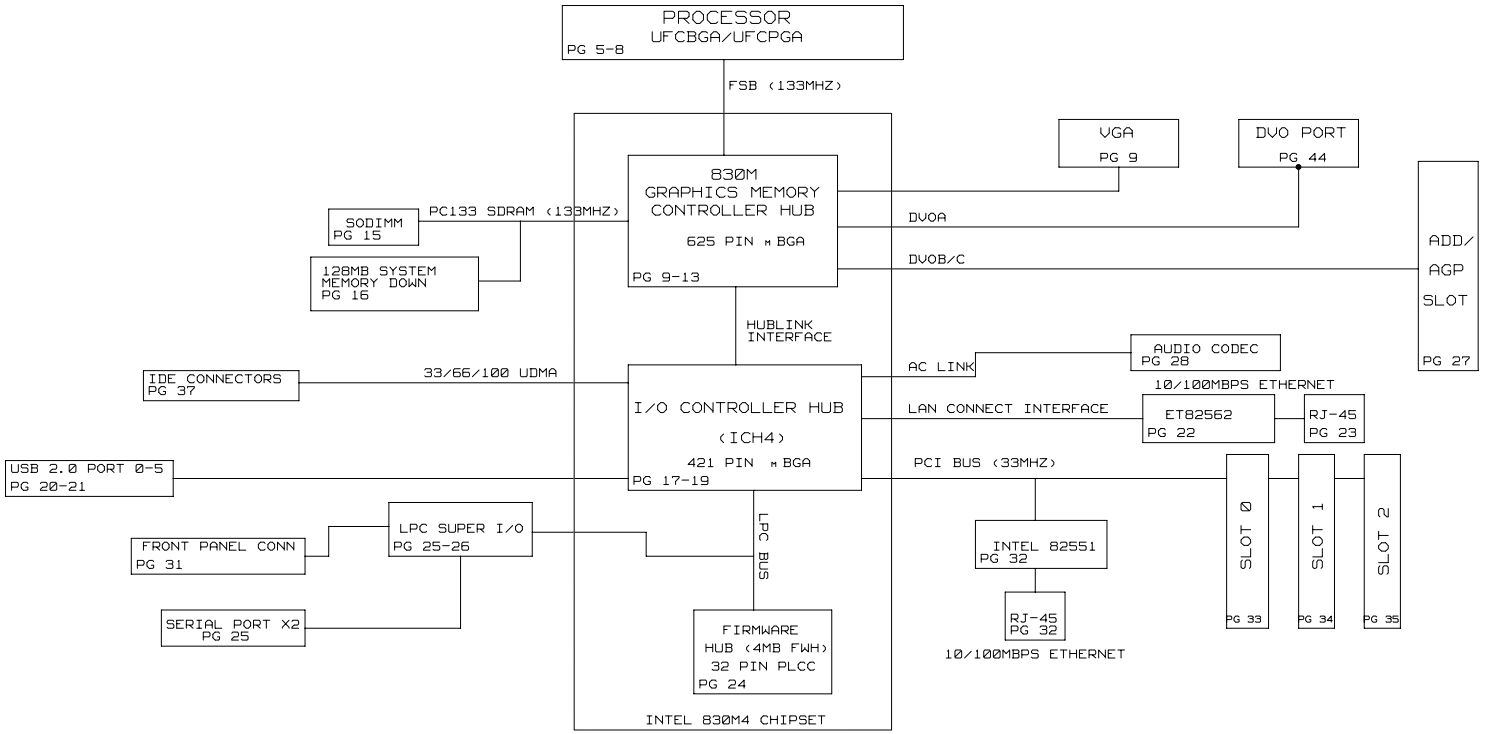
BOM RELEASE DATE		PB NUMBER C68533-004		
SIGNATURE	DATE	intel	5200 NE ELAM YOUNG PARKWAY HILLSBORO, OR 97124-6497	
DRN BY				
CHK BY		TITLE SCH, PBA, 830M4		
ENGR APVD				
APVD			DOCUMENT NUMBER	PAGE 1/52 / REV 1.0
APVD				



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MAINBOARD ARCHITECTURE

	DOCUMENT NUMBER	PAGE	REV
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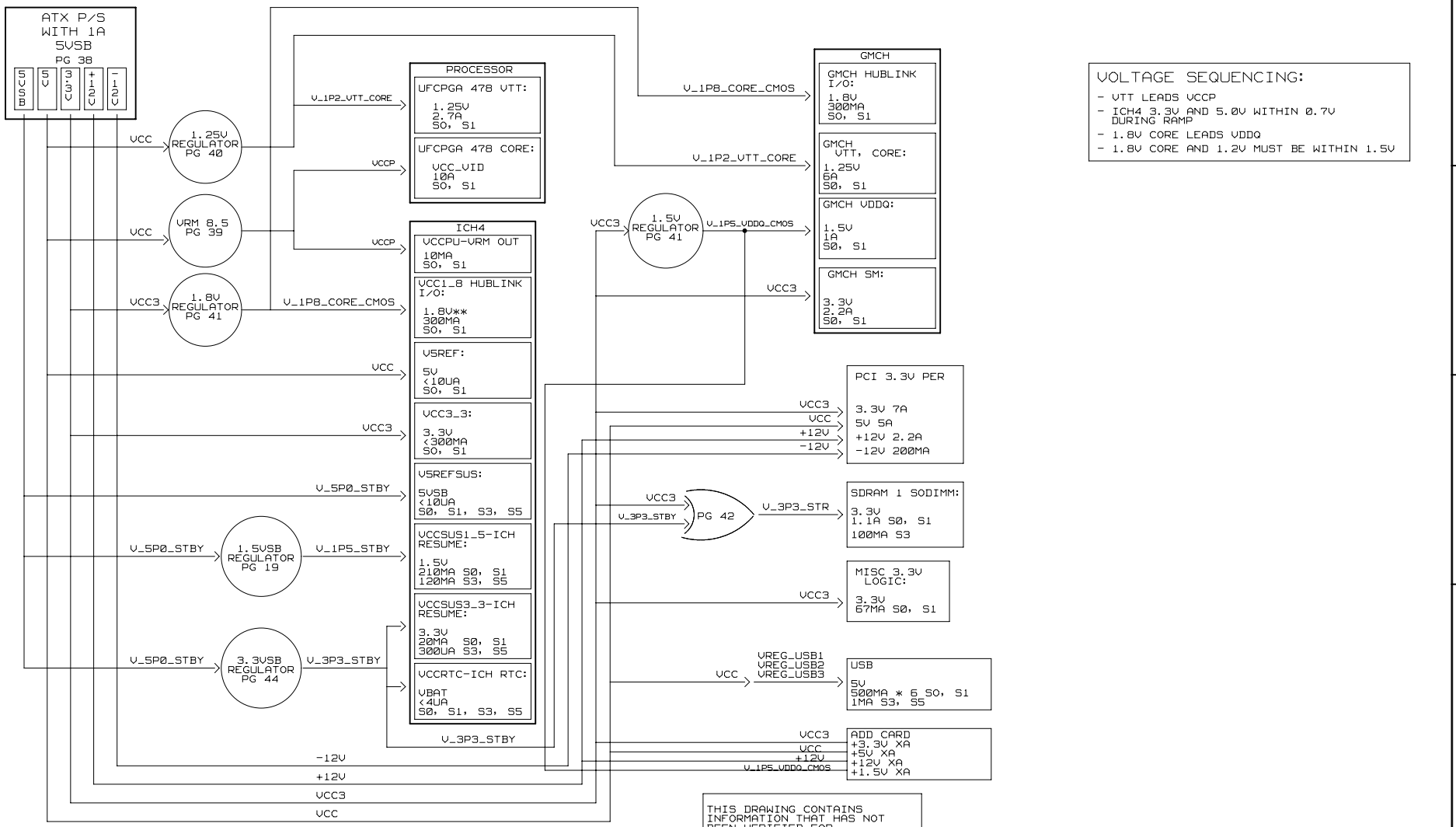

VOLTAGE SEQUENCING:

- VTT LEADS VCCP
- ICH4 3.3V AND 5.0V WITHIN 0.7V DURING RAMP
- 1.8V CORE LEADS VDDQ
- 1.8V CORE AND 1.2V MUST BE WITHIN 1.5V

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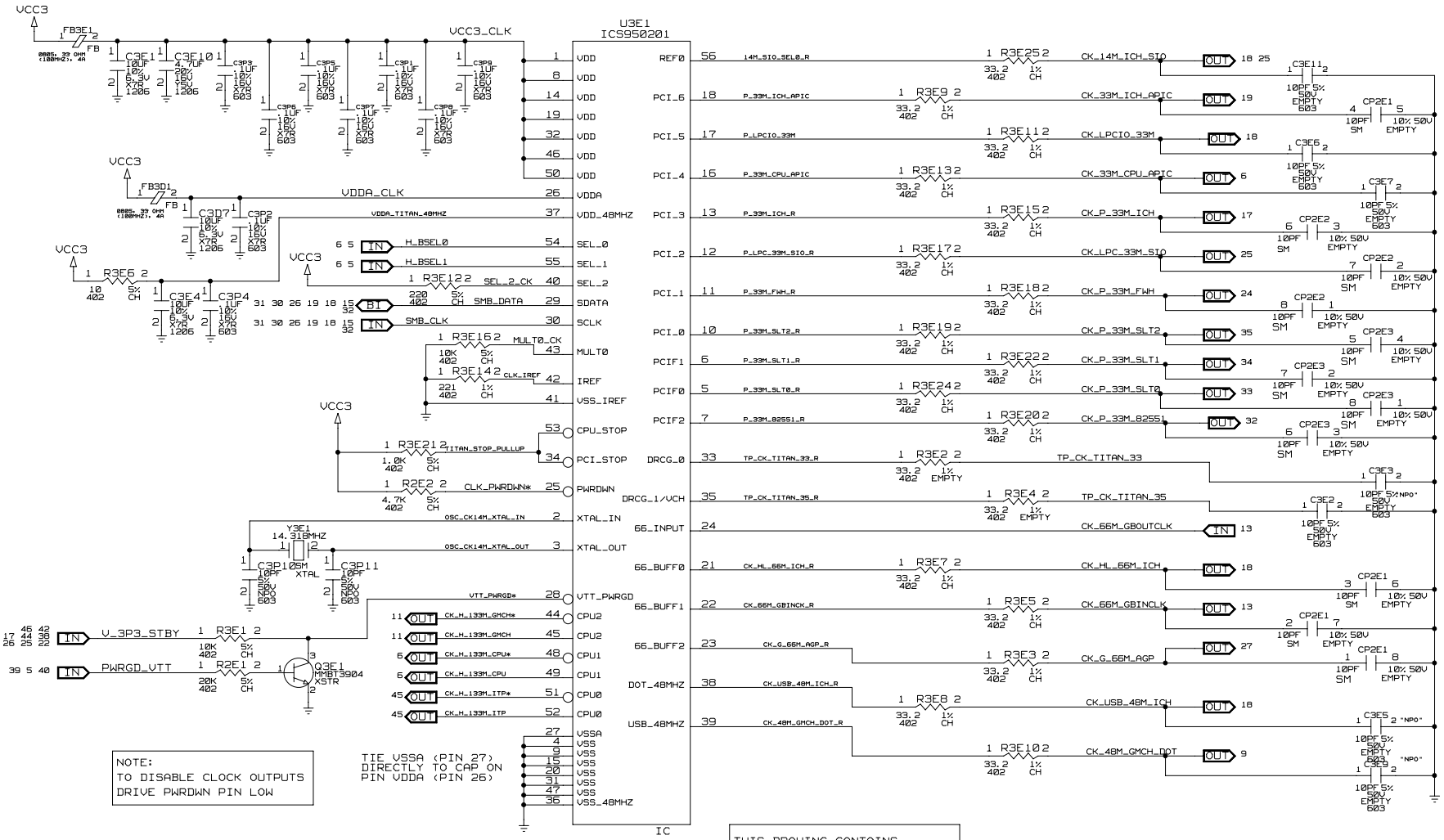
PWR DIAGRAM

DOCUMENT NUMBER	PAGE	REV
	3	1.0


U3E1
ICS950201
VCC3
VCC3_CLK
VDDA_CLK
VDDA_TITAN_48MHZ
H_BSEL0
H_BSEL1
SEL_2_CK
SMB_DATA
SMB_CLK
MULT0_CK
CLK_IREF
TITAN_STOP_PULLUP
CLK_PWRDWN#
OSC_CK14M_XTAL_IN
OSC_CK14M_XTAL_OUT
VTT_PWRGD#
V_3P3_STBY
PWRGD_VTT
CK_H_133M_GMCH#
CK_H_133M_GMCH
CK_H_133M_CPU#
CK_H_133M_CPU
CK_H_133M_ITP#
CK_H_133M_ITP
VDD
VDDA
VDD_48MHZ
SEL_0
SEL_1
SEL_2
SDATA
SCLK
MULT0
IREF
VSS_IREF
CPU_STOP
PCI_STOP
PWRDWN
XTAL_IN
XTAL_OUT
VTT_PWRGD
CPU2
CPU1
CPU0
VSSA
VSS
VSS_48MHZ
REF0
PCI_6
PCI_5
PCI_4
PCI_3
PCI_2
PCI_1
PCI_0
PCIF1
PCIF0
PCIF2
DRCG_0
DRCG_1/VCH
66_INPUT
66_BUFF0
66_BUFF1
66_BUFF2
DOT_48MHZ
USB_48MHZ
IC
14M_SIO_SEL0_R
P_33M_ICH_APIC
P_LPCIO_33M
P_33M_CPU_APIC
P_33M_ICH_R
P_LPC_33M_SIO_R
P_33M_FWH_R
P_33M_SLT2_R
P_33M_SLT1_R
P_33M_SLT0_R
P_33M_8255_R
TP_CK_TITAN_33_R
TP_CK_TITAN_35_R
CK_HL_66M_ICH_R
CK_66M_GBINCK_R
CK_G_66M_AGP_R
CK_USB_48M_ICH_R
CK_48M_GMCH_DOT_R
CK_14M_ICH_SIO
CK_33M_ICH_APIC
CK_LPCIO_33M
CK_33M_CPU_APIC
CK_P_33M_ICH
CK_LPC_33M_SIO
CK_P_33M_FWH
CK_P_33M_SLT2
CK_P_33M_SLT1
CK_P_33M_SLT0
CK_P_33M_8255
TP_CK_TITAN_33
TP_CK_TITAN_35
CK_66M_GBOUTCLK
CK_HL_66M_ICH
CK_66M_GBINCLK
CK_G_66M_AGP
CK_USB_48M_ICH
CK_48M_GMCH_DOT
Y3E1
14.318MHZ
Q3E1
MMBT3904
XSTR
NOTE:
TO DISABLE CLOCK OUTPUTS
DRIVE PWRDWN PIN LOW
TIE VSSA (PIN 27)
DIRECTLY TO CAP ON
PIN VDDA (PIN 26)
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CLOCK GENERATOR
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PAGE
4
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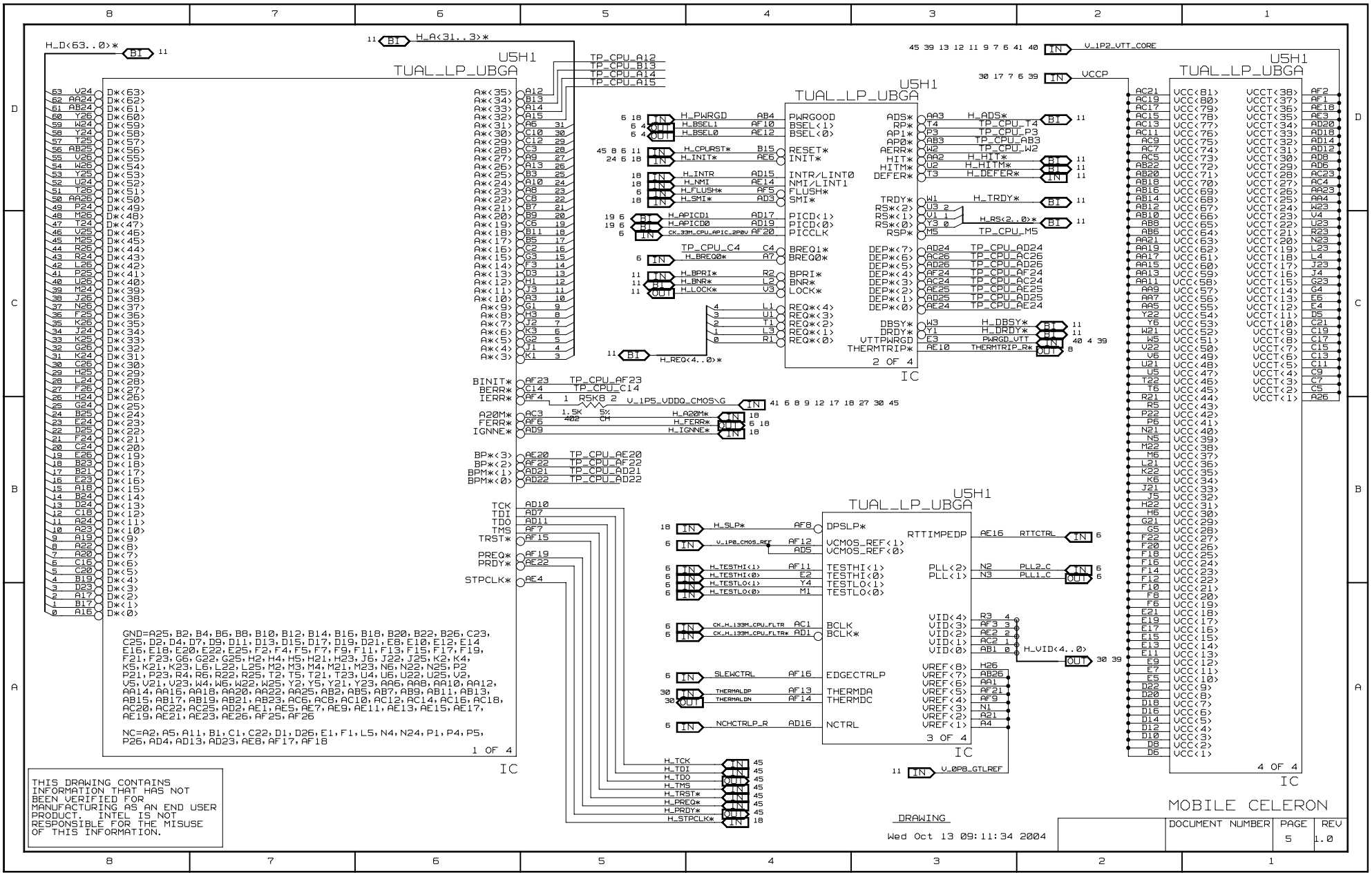
U5H1
TUAL_LP_UBGA
H_D<63..0>*
H_A<31..3>*
H_REQ<4..0>*
TP_CPU_A12
TP_CPU_B13
TP_CPU_A14
TP_CPU_A15
TP_CPU_C4
TP_CPU_AF23
TP_CPU_C14
TP_CPU_AE20
TP_CPU_AF22
TP_CPU_AD21
TP_CPU_AD22
R5K8
V_1P5_VDDQ_CMOS\G
H_A20M*
H_FERR*
H_IGNNE*
H_PWRGD
H_BSEL1
H_BSEL0
H_CPURST*
H_INIT*
H_INTR
H_NMI
H_FLUSH*
H_SMI*
H_APICD1
H_APICD0
CK_33M_CPU_APIC_2P8V
H_BPRI*
H_BNR*
H_LOCK*
H_SLP*
V_1P8_CMOS_REF
H_TESTHI<1>
H_TESTHI<0>
H_TESTLO<1>
H_TESTLO<0>
CK_H_133M_CPU_FLTR
CK_H_133M_CPU_FLTR*
SLEWCTRL
THERMALDP
THERMALDN
NCHCTRLP_R
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST*
H_PREQ*
H_PRDY*
H_STPCLK*
V_1P2_VTT_CORE
VCCP
H_ADS*
H_HIT*
H_HITM*
H_DEFER*
H_TRDY*
H_RS<2..0>*
TP_CPU_M5
H_DBSY*
H_DRDY*
PWRGD_VTT
THERMTRIP_R*
RTTCTRL
PLL2_C
PLL1_C
H_VID<4..0>
V_0P8_GTLREF
GND=A25, B2, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, B26, C23, C25, D2, D4, D7, D9, D11, D13, D15, D17, D19, D21, E8, E10, E12, E14 E16, E18, E20, E22, E25, F2, F4, F5, F7, F9, F11, F13, F15, F17, F19, F21, F23, G6, G22, G25, H2, H4, H5, H21, H23, J6, J22, J25, K2, K4, K5, K21, K23, L6, L22, L25, M2, M3, M4, M21, M23, N6, N22, N25, P2 P21, P23, R4, R6, R22, R25, T2, T5, T21, T23, U4, U6, U22, U25, V2, V5, V21, V23, W4, W6, W22, W25, Y2, Y5, Y21, Y23, AA6, AA8, AA10, AA12, AA14, AA16, AA18, AA20, AA22, AA25, AB2, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB23, AC5, AC8, AC10, AC12, AC14, AC16, AC18, AC20, AC22, AC25, AD2, AE1, AE5, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE21, AE23, AE26, AF25, AF26
NC=A2, A5, A11, B1, C1, C22, D1, D26, E1, F1, L5, N4, N24, P1, P4, P5, P26, AD4, AD13, AD23, AE8, AF17, AF18
1 OF 4
2 OF 4
3 OF 4
4 OF 4
IC
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MOBILE CELERON
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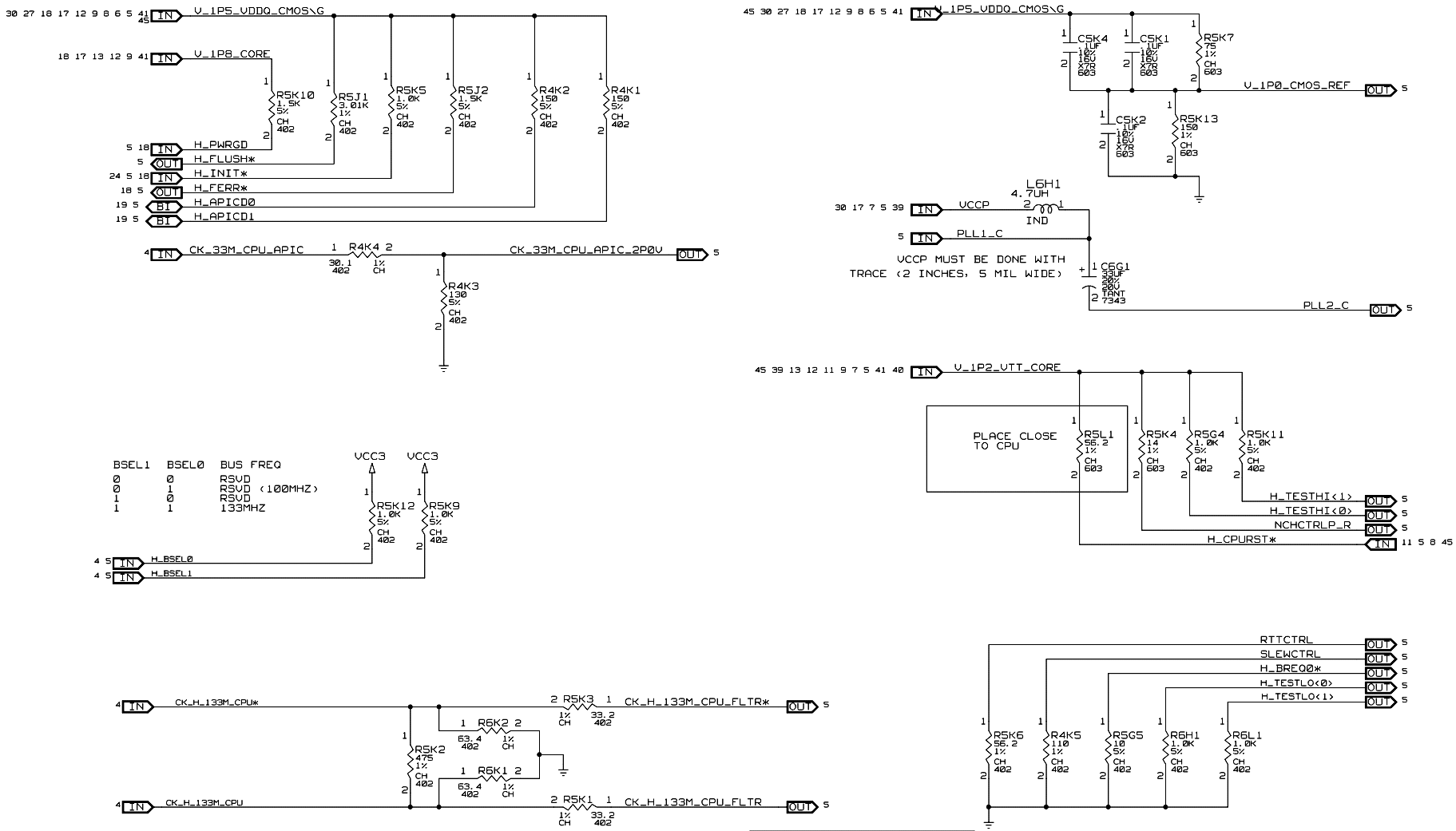

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MOBILE CELERON PULLUPS

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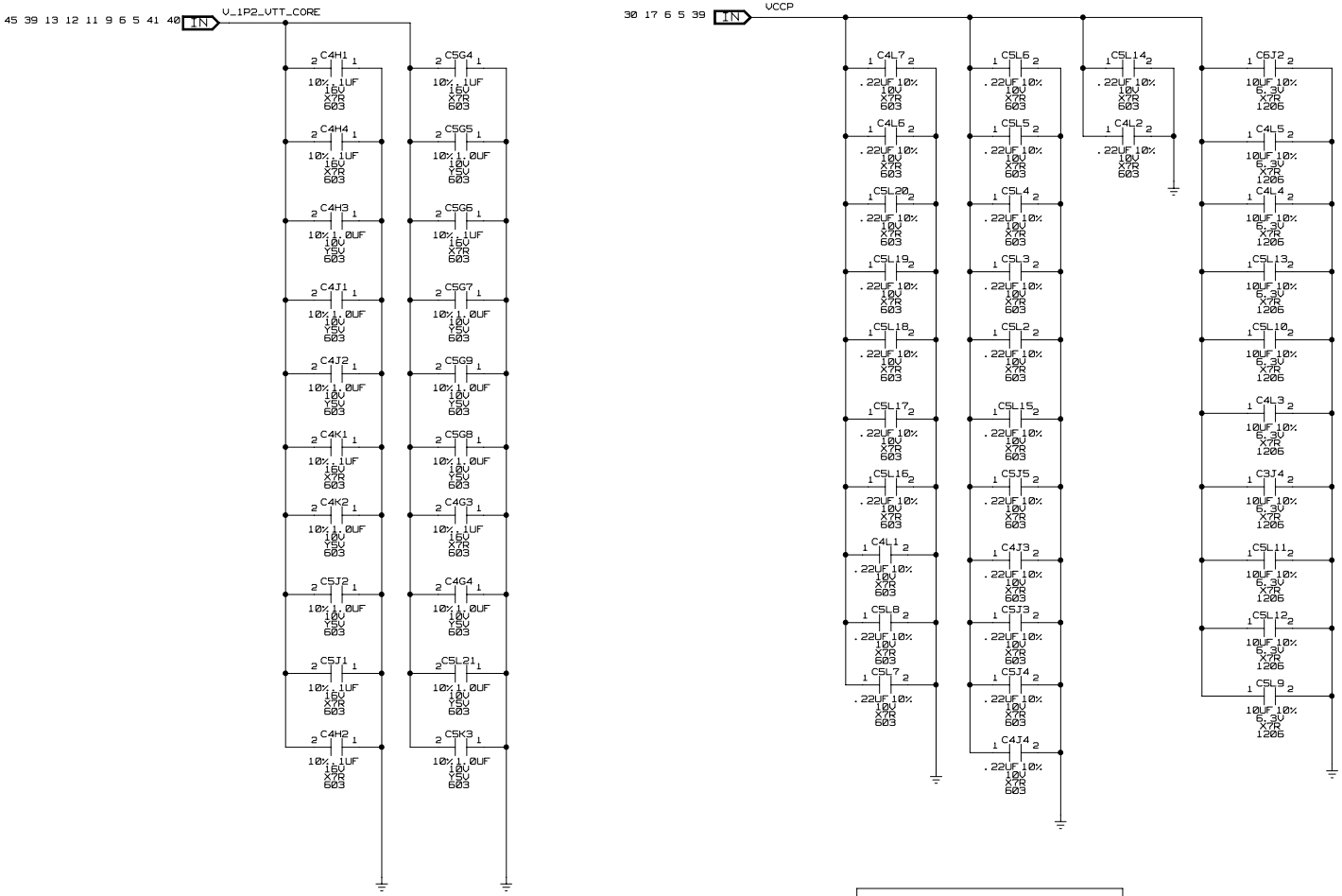

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CPU CAPS

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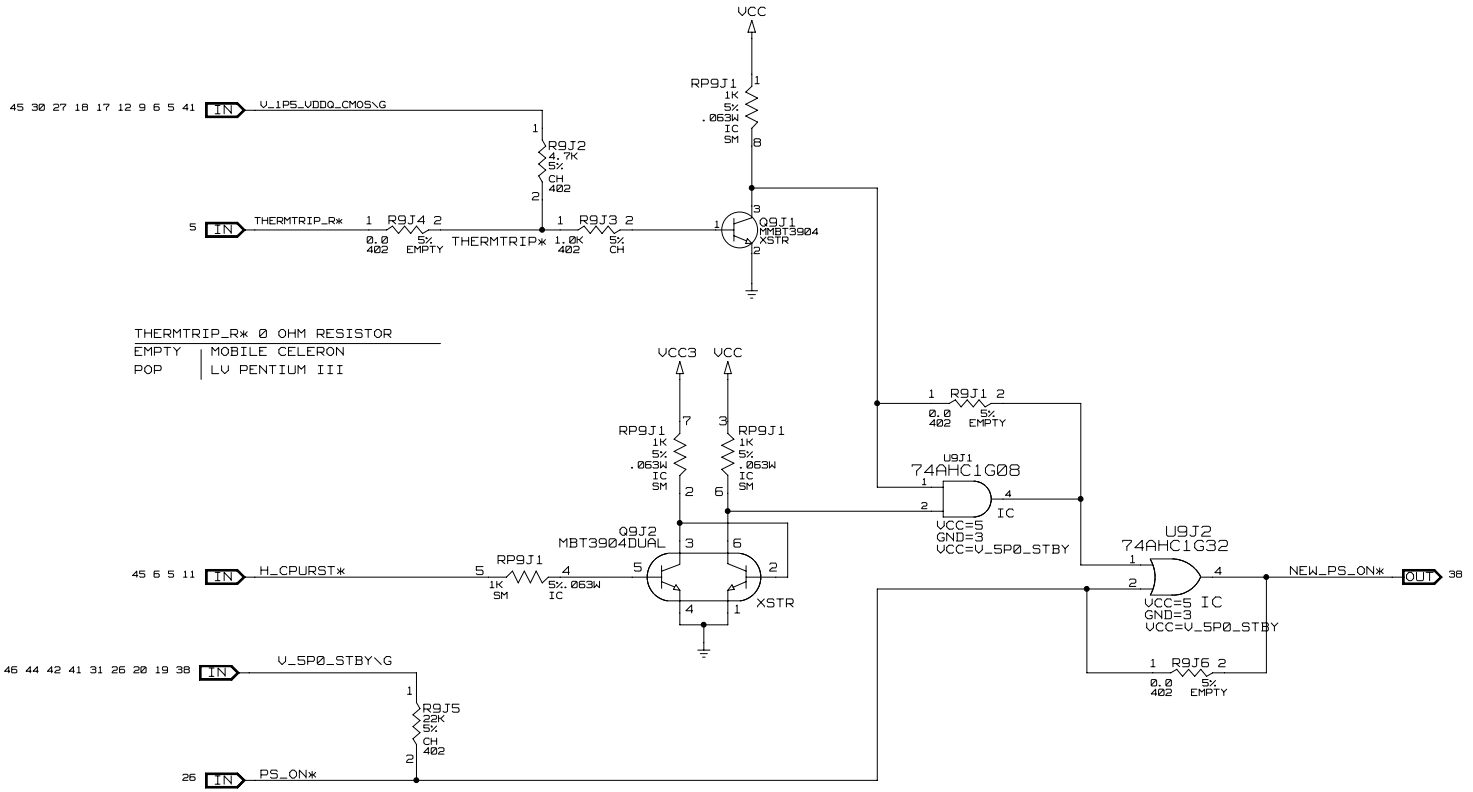

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THERMTRIP

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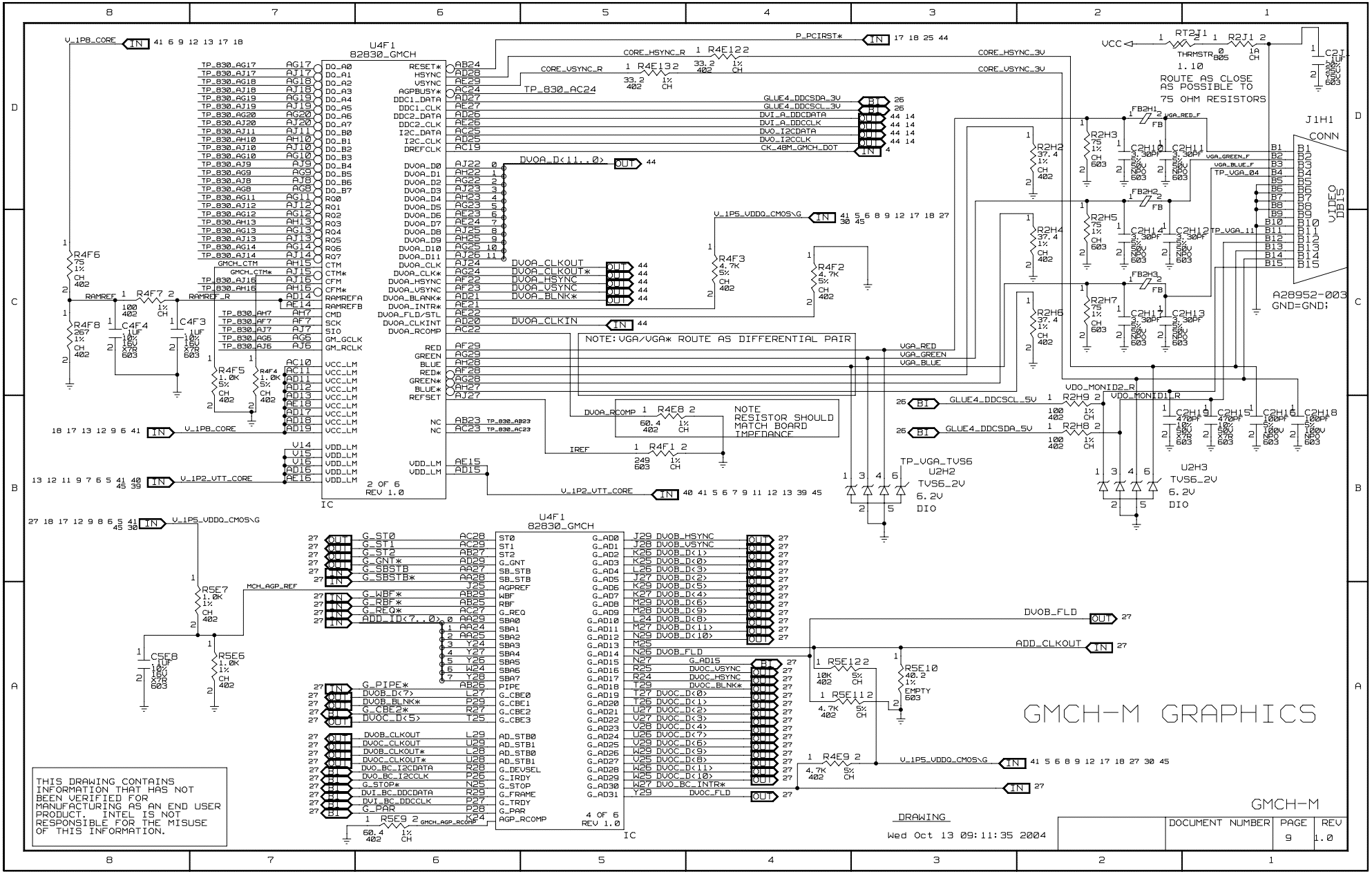
U4F1
82830_GMCH
IC
2 OF 6
REV 1.0
4 OF 6
REV 1.0
NOTE: VGA/VGA* ROUTE AS DIFFERENTIAL PAIR
NOTE
RESISTOR SHOULD
MATCH BOARD
IMPEDANCE
ROUTE AS CLOSE
AS POSSIBLE TO
75 OHM RESISTORS
1.10
TP_VGA_TVS6
U2H2
TVS6_2V
6.2V
DIO
U2H3
TVS6_2V
6.2V
DIO
J1H1
CONN
VIDEO
DB15
A28952-003
GND=GND;
GMCH-M GRAPHICS
GMCH-M
DRAWING
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9
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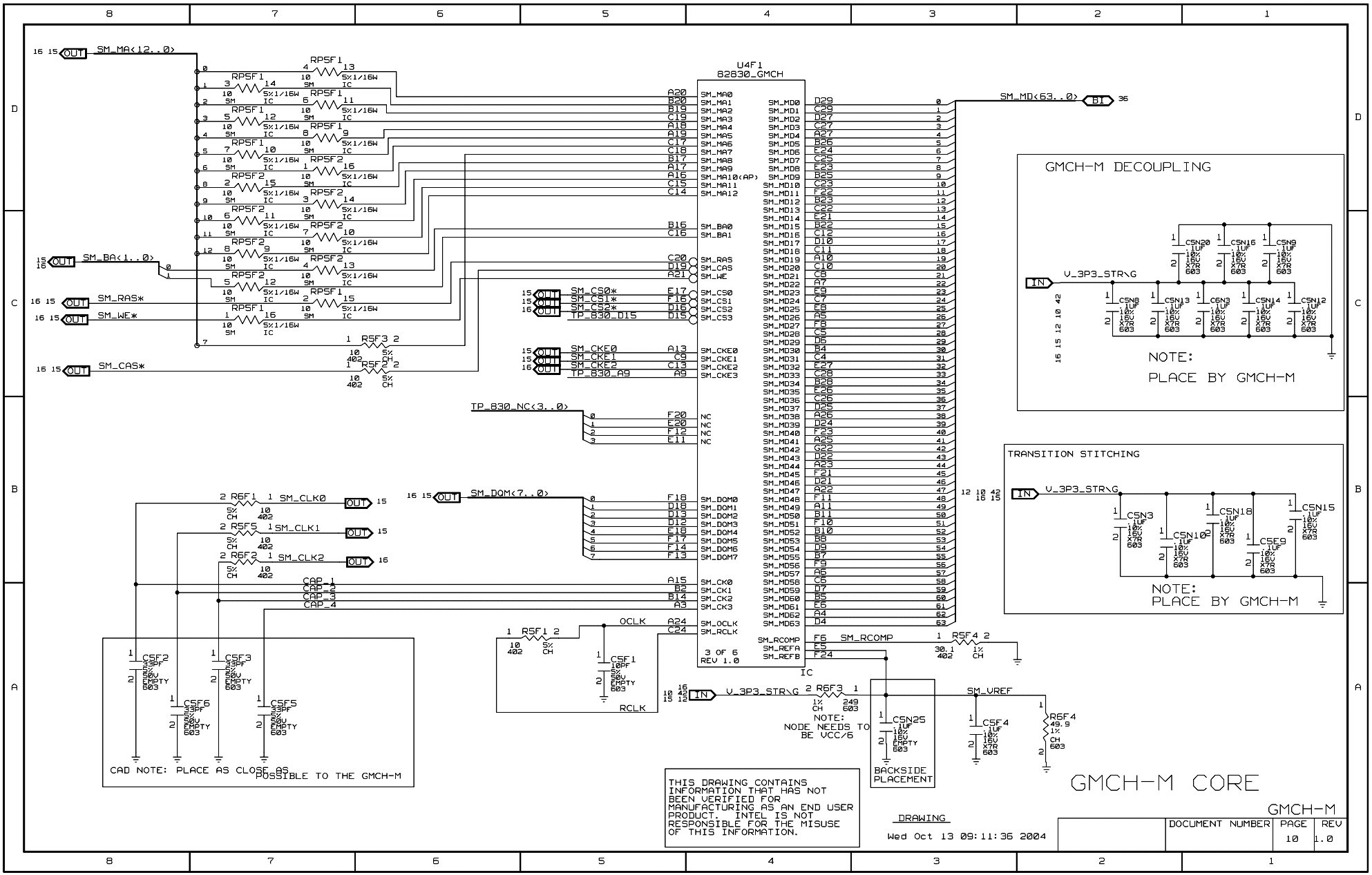
U4F1
82830_GMCH
SM_MA<12..0>
SM_BA<1..0>
SM_RAS*
SM_WE*
SM_CAS*
SM_CS0*
SM_CS1*
SM_CS2*
SM_CKE0
SM_CKE1
SM_CKE2
SM_DQM<7..0>
SM_CLK0
SM_CLK1
SM_CLK2
SM_MD<63..0>
SM_RCOMP
SM_VREF
OCLK
RCLK
V_3P3_STR\G
TP_830_NC<3..0>
TP_830_A9
TP_830_D15
3 OF 6
REV 1.0
IC
GMCH-M DECOUPLING
NOTE:
PLACE BY GMCH-M
TRANSITION STITCHING
NOTE:
PLACE BY GMCH-M
CAD NOTE: PLACE AS CLOSE AS POSSIBLE TO THE GMCH-M
NOTE:
NODE NEEDS TO
BE VCC/6
BACKSIDE
PLACEMENT
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GMCH-M CORE
GMCH-M
DOCUMENT NUMBER
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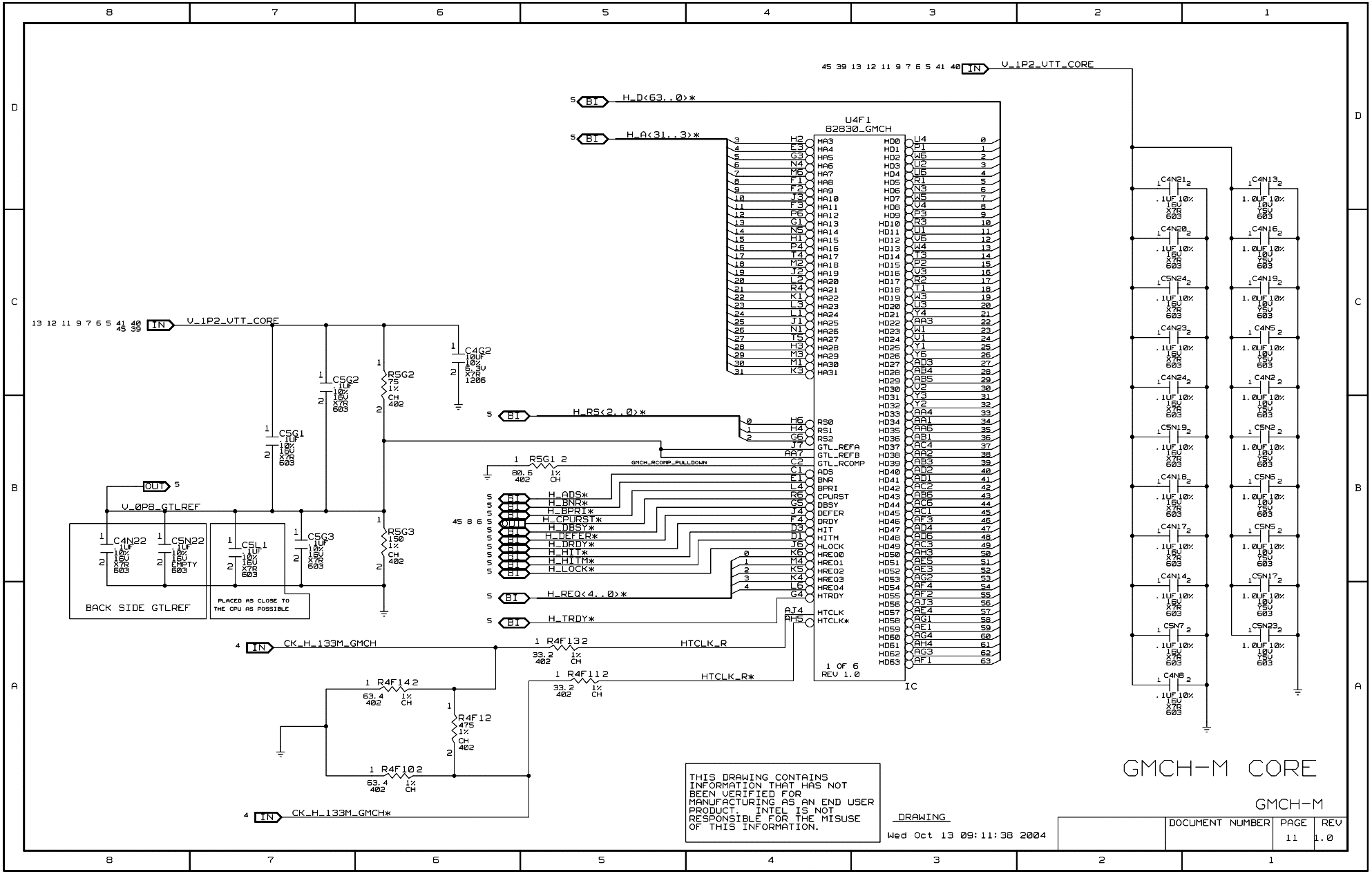
V_1P2_VTT_CORE
H_D<63..0>*
H_A<31..3>*
U4F1
82830_GMCH
H_RS<2..0>*
GMCH_RCOMP_PULLDOWN
H_ADS*
H_BNR*
H_BPRI*
H_CPURST*
H_DBSY*
H_DEFER*
H_DRDY*
H_HIT*
H_HITM*
H_LOCK*
H_REQ<4..0>*
H_TRDY*
V_0P8_GTLREF
BACK SIDE GTLREF
PLACED AS CLOSE TO THE CPU AS POSSIBLE
CK_H_133M_GMCH
CK_H_133M_GMCH*
HTCLK_R
HTCLK_R*
1 OF 6
REV 1.0
IC
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GMCH-M CORE
GMCH-M
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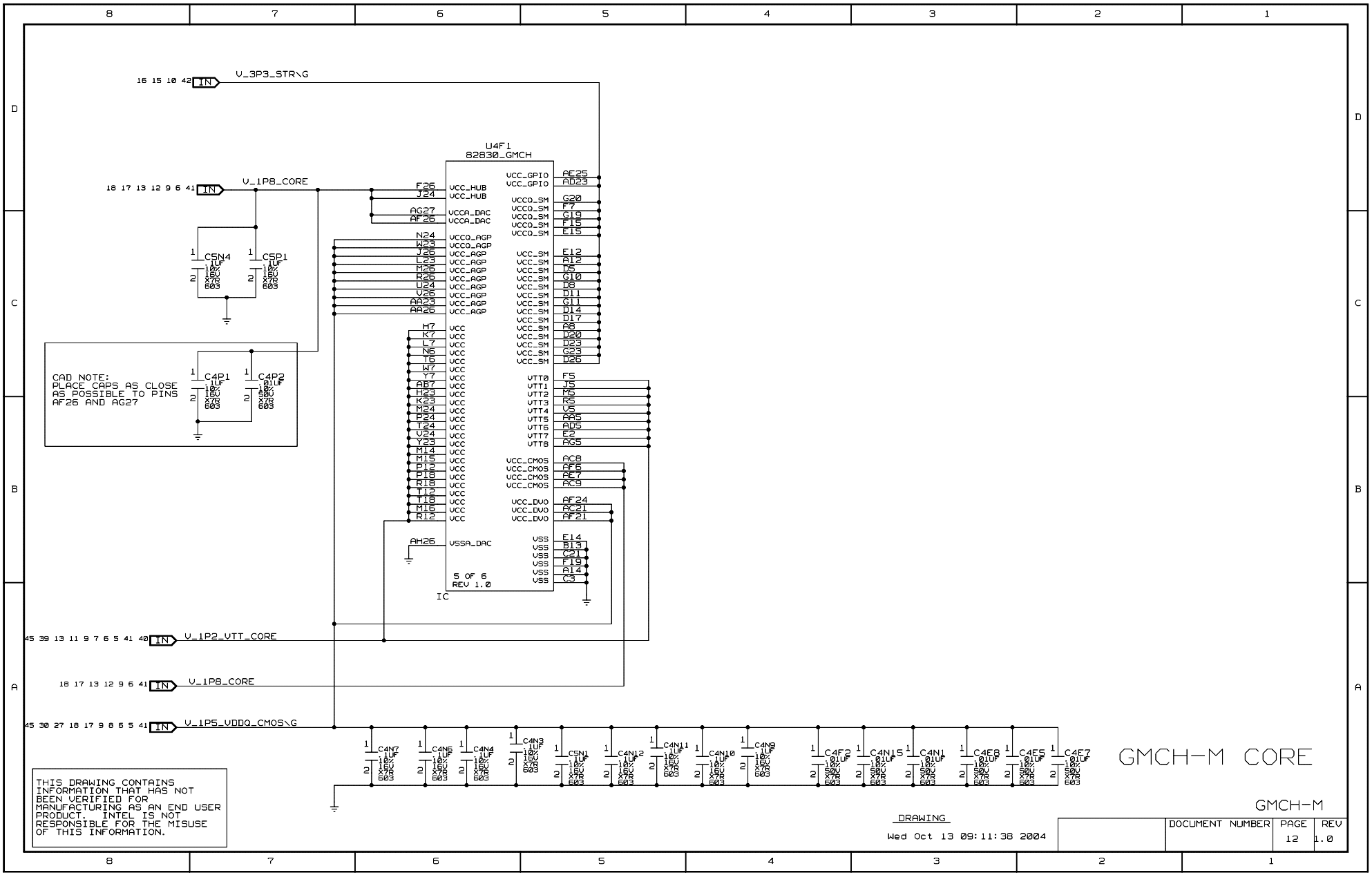
V_3P3_STR\G
16 15 10 42
IN
U4F1
82830_GMCH
V_1P8_CORE
18 17 13 12 9 6 41
C5N4
C5P1
CAD NOTE:
PLACE CAPS AS CLOSE
AS POSSIBLE TO PINS
AF26 AND AG27
C4P1
C4P2
F26 VCC_HUB
J24 VCC_HUB
AG27 VCCA_DAC
AF26 VCCA_DAC
N24 VCCQ_AGP
W23 VCCQ_AGP
J26 VCC_AGP
L23 VCC_AGP
M26 VCC_AGP
R25 VCC_AGP
U24 VCC_AGP
V26 VCC_AGP
AA23 VCC_AGP
AA26 VCC_AGP
H7 VCC
K7 VCC
L7 VCC
N6 VCC
T6 VCC
W7 VCC
Y7 VCC
AB7 VCC
H23 VCC
K23 VCC
M24 VCC
P24 VCC
T24 VCC
V24 VCC
Y23 VCC
M14 VCC
M15 VCC
P12 VCC
P18 VCC
R18 VCC
T12 VCC
T18 VCC
M16 VCC
R12 VCC
AM26 VSSA_DAC
5 OF 6
REV 1.0
IC
VCC_GPIO AF25
VCC_GPIO AD23
VCCQ_SM G20
VCCQ_SM F7
VCCQ_SM G19
VCCQ_SM F15
VCCQ_SM E15
VCC_SM E12
VCC_SM A12
VCC_SM D5
VCC_SM G10
VCC_SM D8
VCC_SM D11
VCC_SM G11
VCC_SM D14
VCC_SM D17
VCC_SM A8
VCC_SM D20
VCC_SM D23
VCC_SM G23
VCC_SM D26
VTT0 F5
VTT1 J5
VTT2 M5
VTT3 R5
VTT4 V5
VTT5 AA5
VTT6 AD5
VTT7 E2
VTT8 AG5
VCC_CMOS AC8
VCC_CMOS AF6
VCC_CMOS AF7
VCC_CMOS AC9
VCC_DVO AF24
VCC_DVO AC21
VCC_DVO AF21
VSS F14
VSS B13
VSS C21
VSS F19
VSS A14
VSS C3
45 39 13 11 9 7 6 5 41 40
V_1P2_VTT_CORE
V_1P8_CORE
45 30 27 18 17 9 8 6 5 41
V_1P5_VDDQ_CMOS\G
C4N7
C4N6
C4N4
C4N3
C5N1
C4N12
C4N11
C4N10
C4N9
C4F3
C4N15
C4N1
C4E8
C4E5
C4E7
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GMCH-M CORE
GMCH-M
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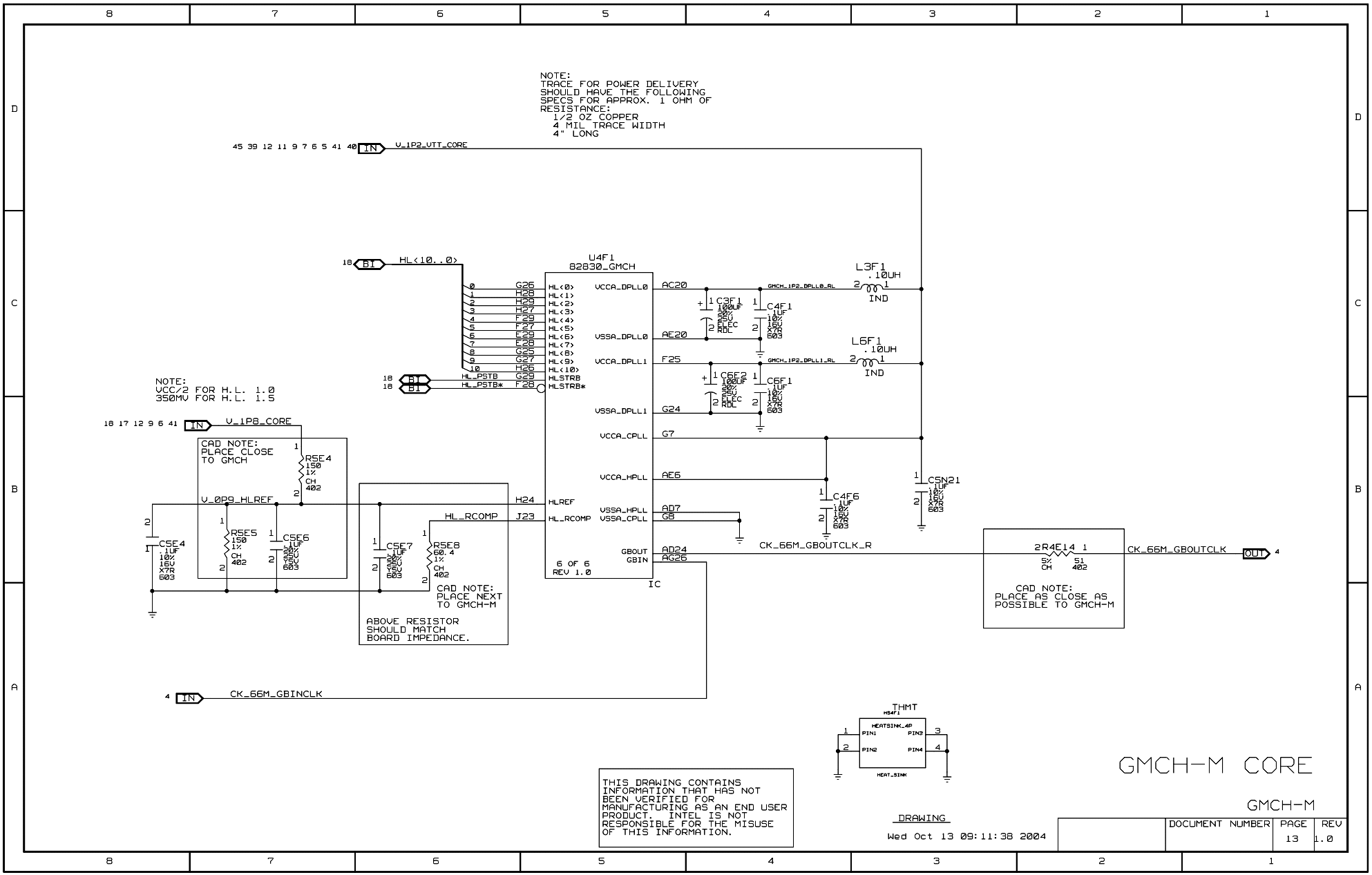
NOTE:
TRACE FOR POWER DELIVERY
SHOULD HAVE THE FOLLOWING
SPECS FOR APPROX. 1 OHM OF
RESISTANCE:
1/2 OZ COPPER
4 MIL TRACE WIDTH
4" LONG
45 39 12 11 9 7 6 5 41 40
IN
V_1P2_VTT_CORE
18
BI
HL<10..0>
U4F1
82830_GMCH
HL<0>
HL<1>
HL<2>
HL<3>
HL<4>
HL<5>
HL<6>
HL<7>
HL<8>
HL<9>
HL<10>
HLSTRB
HLSTRB#
HL_PSTB
HL_PSTB#
VCCA_DPLL0
VSSA_DPLL0
VCCA_DPLL1
VSSA_DPLL1
VCCA_CPLL
VCCA_HPLL
VSSA_HPLL
VSSA_CPLL
HLREF
HL_RCOMP
GBOUT
GBIN
AC20
AE20
F25
G24
G7
AE6
AD7
G8
AD24
AG26
H24
J23
6 OF 6
REV 1.0
IC
L3F1
.10UH
IND
L6F1
.10UH
IND
GMCH_1P2_DPLL0_RL
GMCH_1P2_DPLL1_RL
C3F1
100UF
C4F1
C6F2
C6F1
C4F6
C5N21
NOTE:
VCC/2 FOR H.L. 1.0
350MV FOR H.L. 1.5
18 17 12 9 6 41
IN
V_1P8_CORE
CAD NOTE:
PLACE CLOSE
TO GMCH
R5E4
150
1%
CH
402
V_0P9_HLREF
R5E5
150
1%
CH
402
C5E6
C5E4
1UF
10%
16V
X7R
603
C5E7
R5E8
60.4
1%
CH
402
HL_RCOMP
CAD NOTE:
PLACE NEXT
TO GMCH-M
ABOVE RESISTOR
SHOULD MATCH
BOARD IMPEDANCE.
CK_66M_GBOUTCLK_R
2R4E14
5%
CH
51
402
CK_66M_GBOUTCLK
OUT
4
CAD NOTE:
PLACE AS CLOSE AS
POSSIBLE TO GMCH-M
4
IN
CK_66M_GBINCLK
THMT
HS4F1
HEATSINK_4P
PIN1
PIN2
PIN3
PIN4
HEAT_SINK
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GMCH-M CORE
GMCH-M
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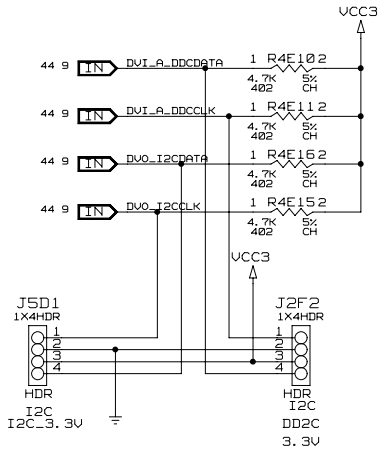


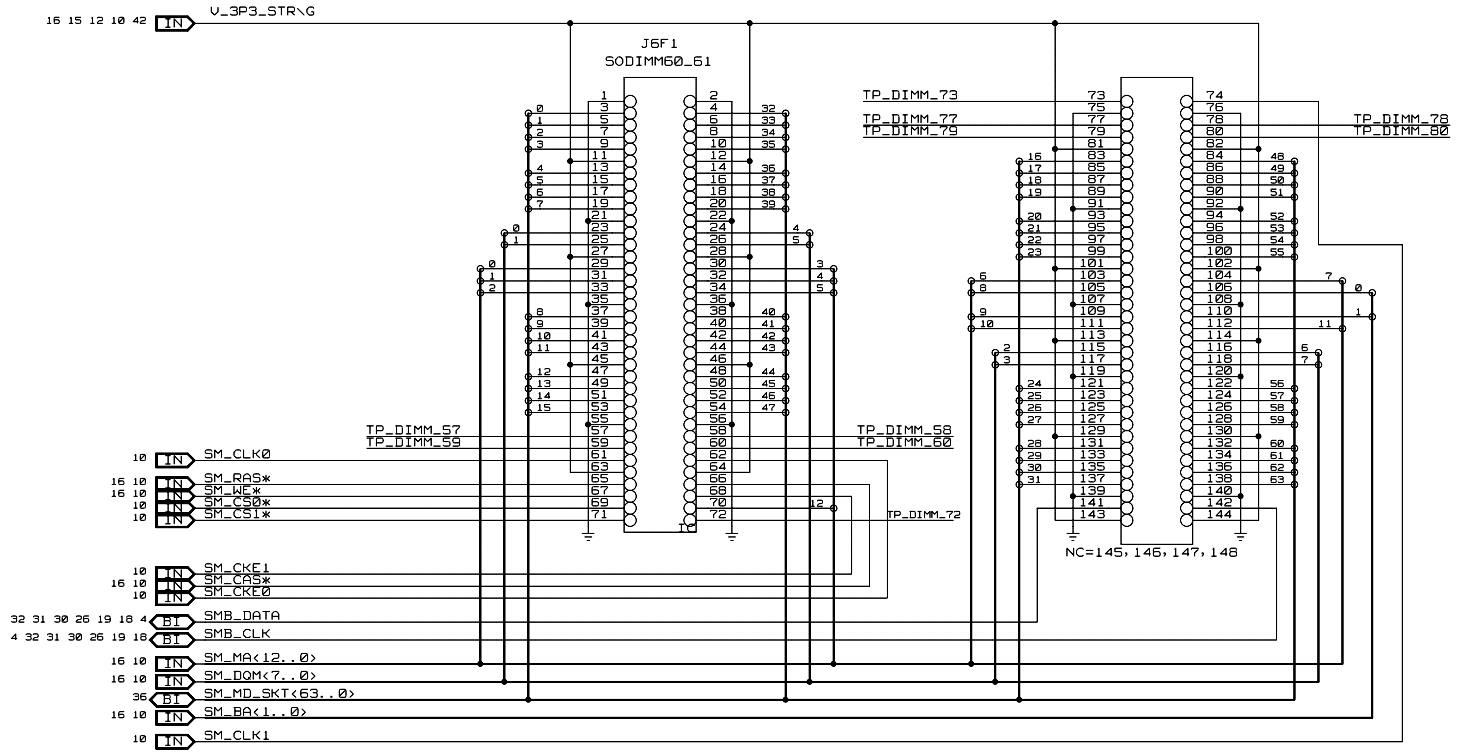
DRAWING

Wed Oct 13 09:11:40 2004

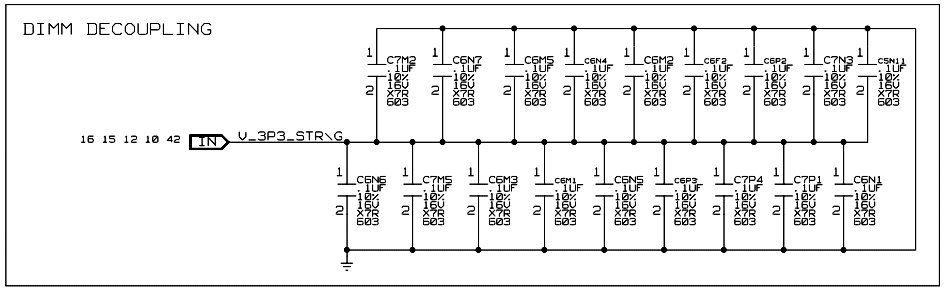
I2C PULLUPS

	DOCUMENT NUMBER	PAGE	REV
		14	1.0

SODIMM 0



DIMM DECOUPLING

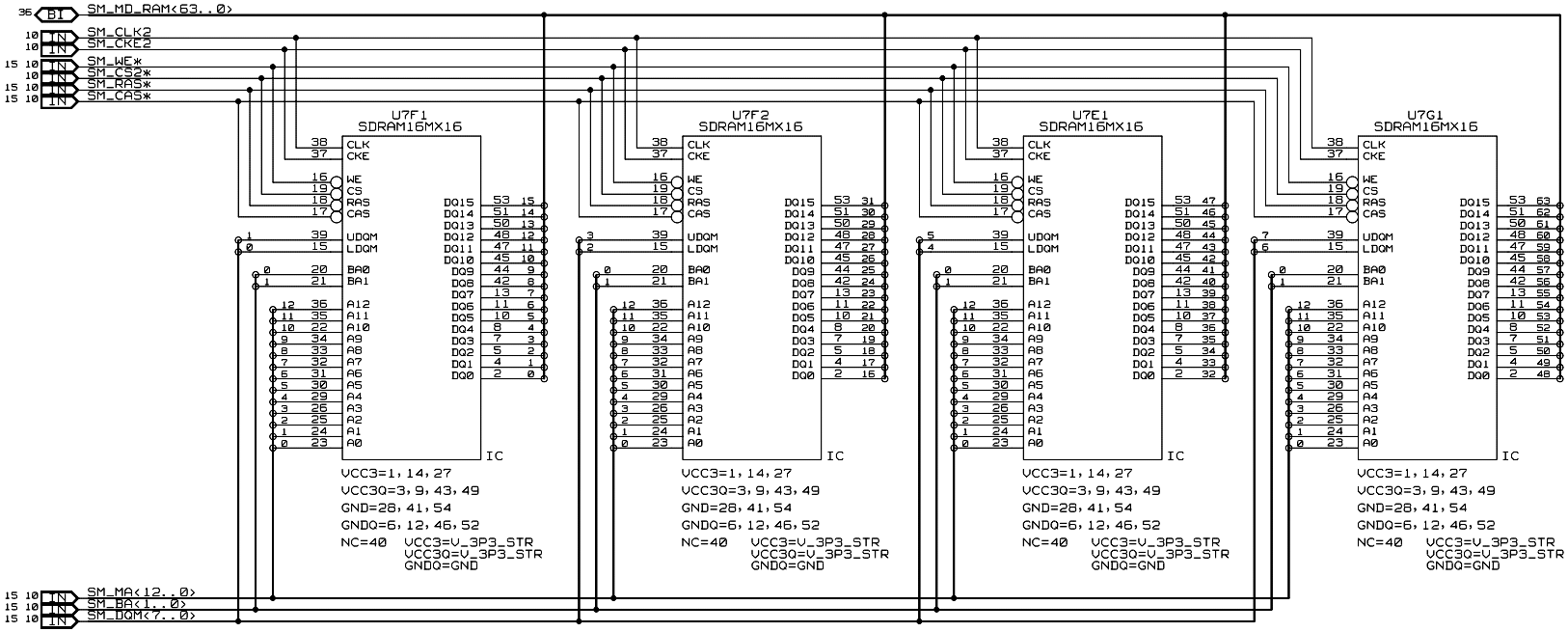


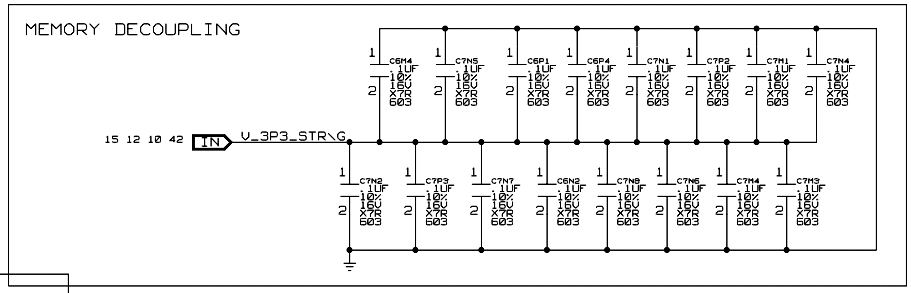
DRAWING

Wed Oct 13 09:11:40 2004

SODIMM CONNECTOR

DOCUMENT NUMBER	PAGE	REV
	15	1.0





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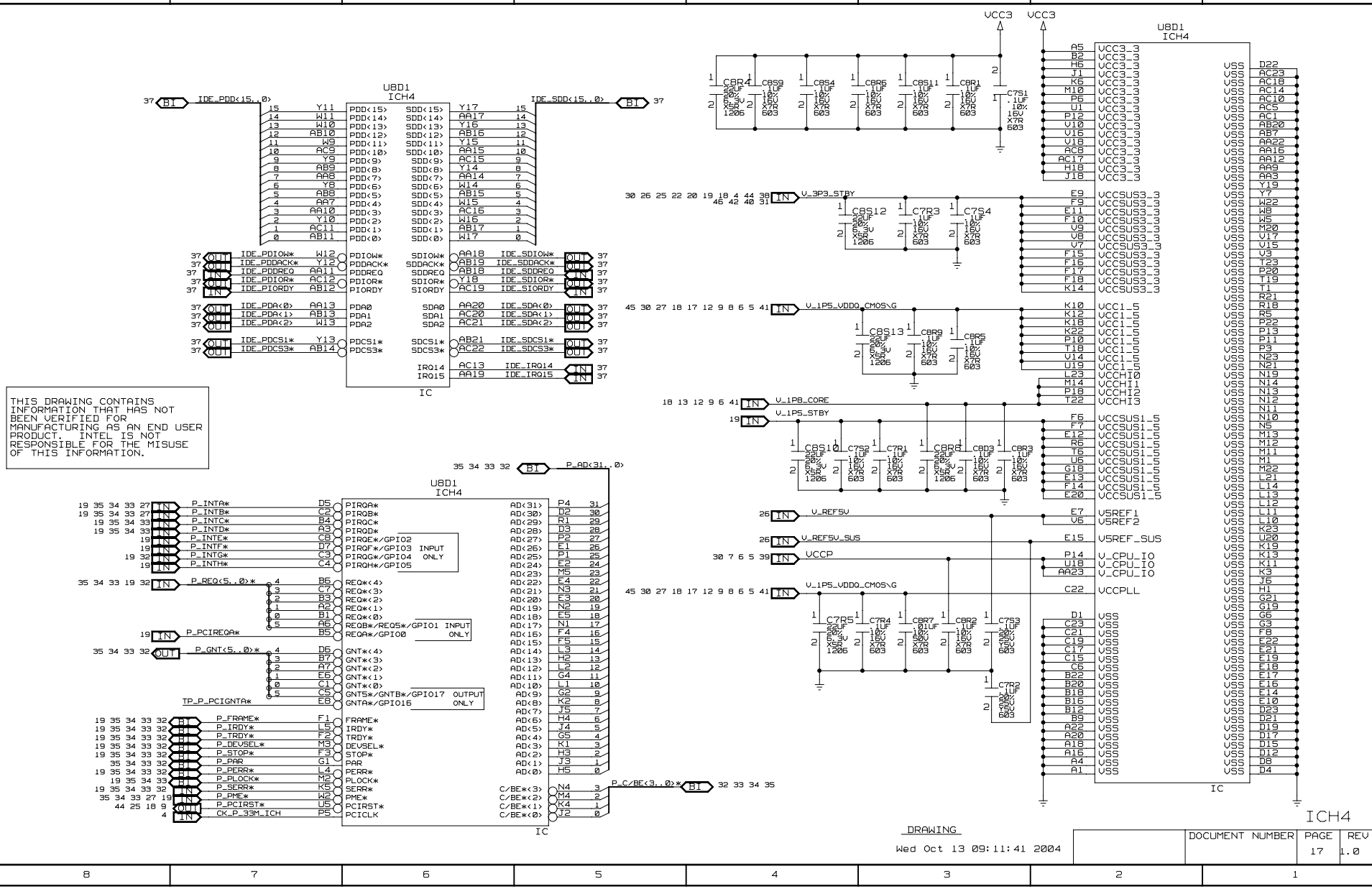
128MB 133MHZ SDRAM

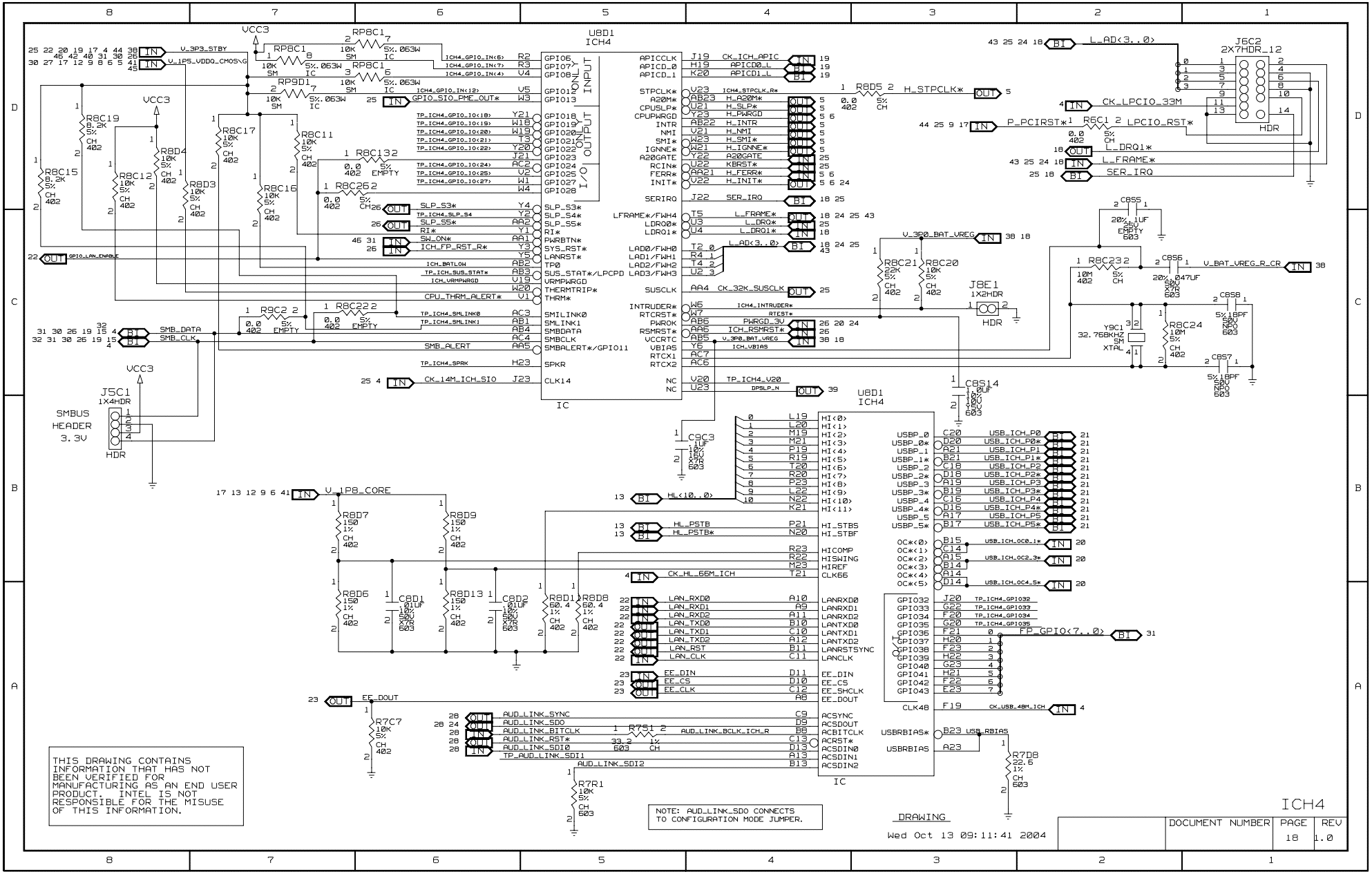
SYSTEM MEMORY - DOWN

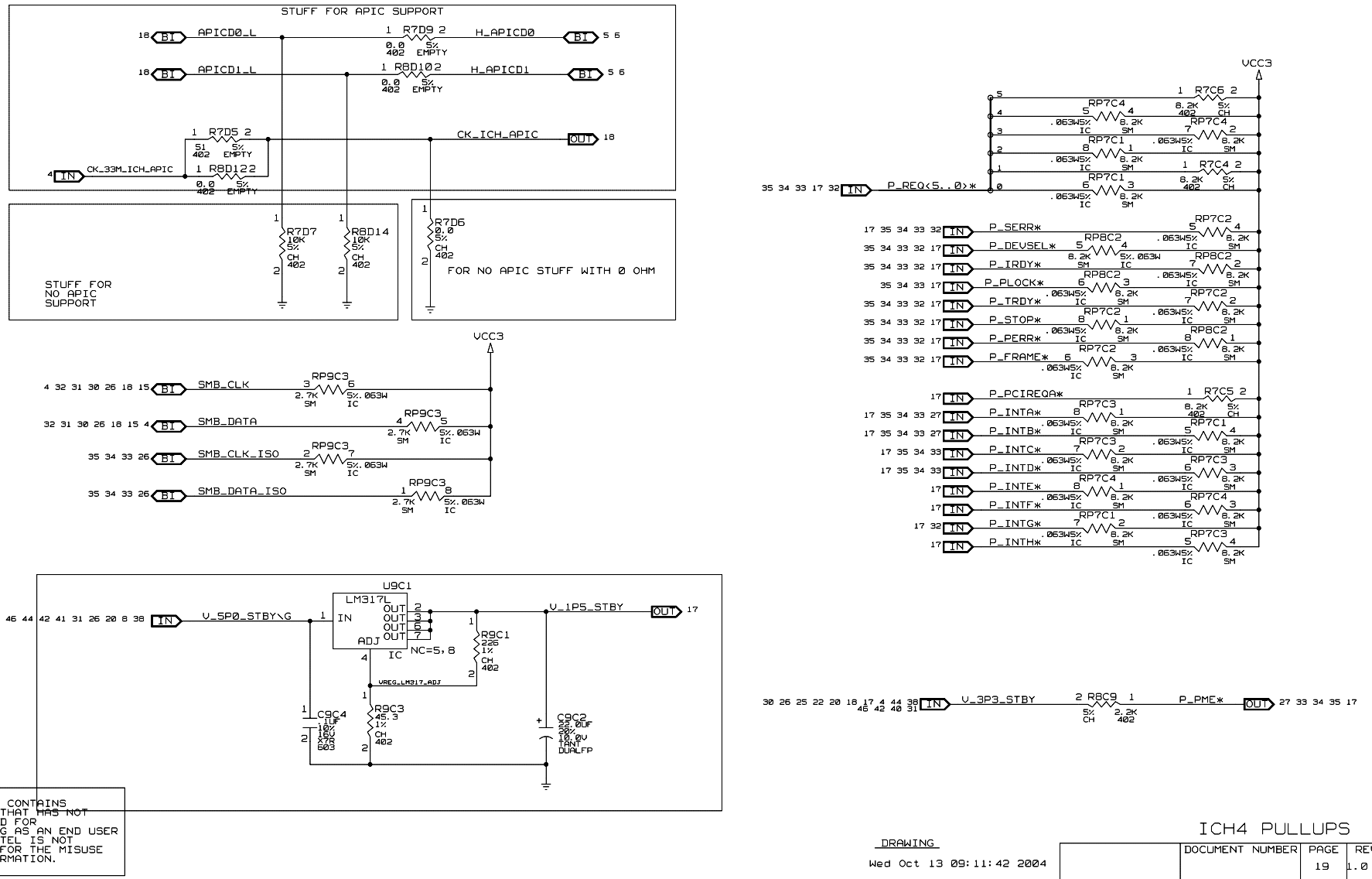
DRAWING

Wed Oct 13 09:11:41 2004

DOCUMENT NUMBER	PAGE	REV
	16	1.0


U8D1
ICH4
IDE_PDD<15..0>
IDE_SDD<15..0>
IDE_PDIOW*
IDE_PDDACK*
IDE_PDDREQ
IDE_PDIOR*
IDE_PIORDY
IDE_PDA<0>
IDE_PDA<1>
IDE_PDA<2>
IDE_PDCS1*
IDE_PDCS3*
IDE_SDIOW*
IDE_SDDACK*
IDE_SDDREQ
IDE_SDIOR*
IDE_SIORDY
IDE_SDA<0>
IDE_SDA<1>
IDE_SDA<2>
IDE_SDCS1*
IDE_SDCS3*
IDE_IRQ14
IDE_IRQ15
IC
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
P_AD<31..0>
P_INTA*
P_INTB*
P_INTC*
P_INTD*
P_INTE*
P_INTF*
P_INTG*
P_INTH*
PIRQA*
PIRQB*
PIRQC*
PIRQD*
PIRQE*/GPIO2
PIRQF*/GPIO3 INPUT
PIRQG*/GPIO4 ONLY
PIRQH*/GPIO5
P_REQ<5..0>*
REQA*/GPIO0 ONLY
REQB*/REQ5*/GPIO1 INPUT
P_PCIREQA*
P_GNT<5..0>*
GNTA*/GPIO16 ONLY
GNT5*/GNTB*/GPIO17 OUTPUT
TP_P_PCIGNTA*
P_FRAME*
P_IRDY*
P_TRDY*
P_DEVSEL*
P_STOP*
P_PAR
P_PERR*
P_PLOCK*
P_SERR*
P_PME*
P_PCIRST*
CK_P_33M_ICH
P_C/BE<3..0>*
VCC3
VCC3_3
VCCSUS3_3
V_3P3_STBY
V_1P5_VDDQ_CMOS\G
V_1P8_CORE
V_1P5_STBY
VCCSUS1_5
V_REF5V
V_REF5V_SUS
VCCP
V_CPU_IO
VCCPLL
VCC1_5
VCCHI0
VCCHI1
VCCHI2
VCCHI3
V5REF1
V5REF2
V5REF_SUS
VSS
ICH4
DRAWING
Wed Oct 13 09:11:41 2004
DOCUMENT NUMBER
PAGE
17
REV
1.0


U8D1
ICH4
IC
J5C1
1X4HDR
SMBUS
HEADER
3.3V
HDR
J6C2
2X7HDR_12
J8E1
1X2HDR
Y9C1
32.768KHZ
XTAL
U8D1
ICH4
IC
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
NOTE: AUD_LINK_SDO CONNECTS TO CONFIGURATION MODE JUMPER.
DRAWING
Wed Oct 13 09:11:41 2004
ICH4
DOCUMENT NUMBER
PAGE
18
REV
1.0



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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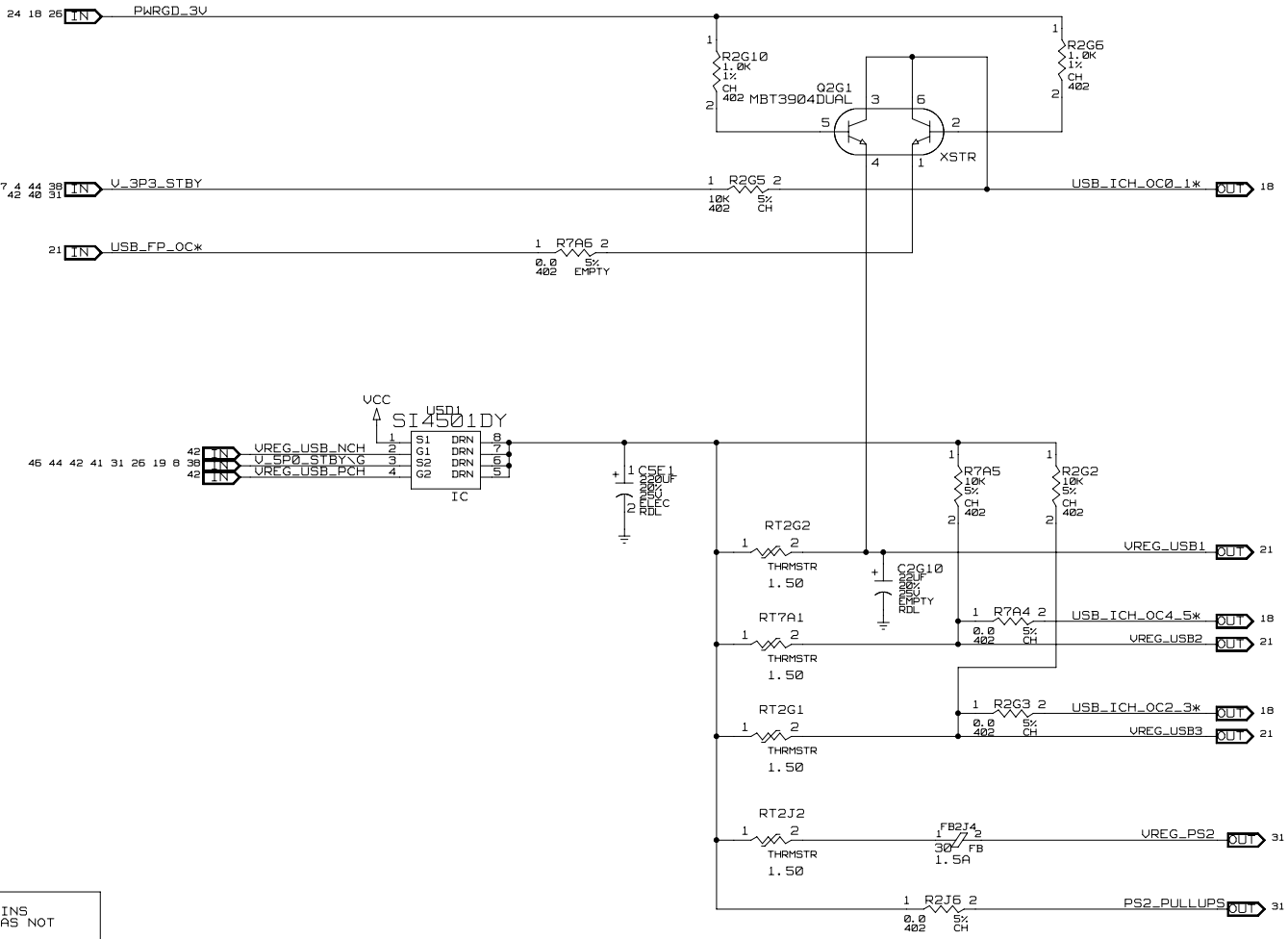
ICH4 PULLUPS

DOCUMENT NUMBER	PAGE	REV
	19	1.0



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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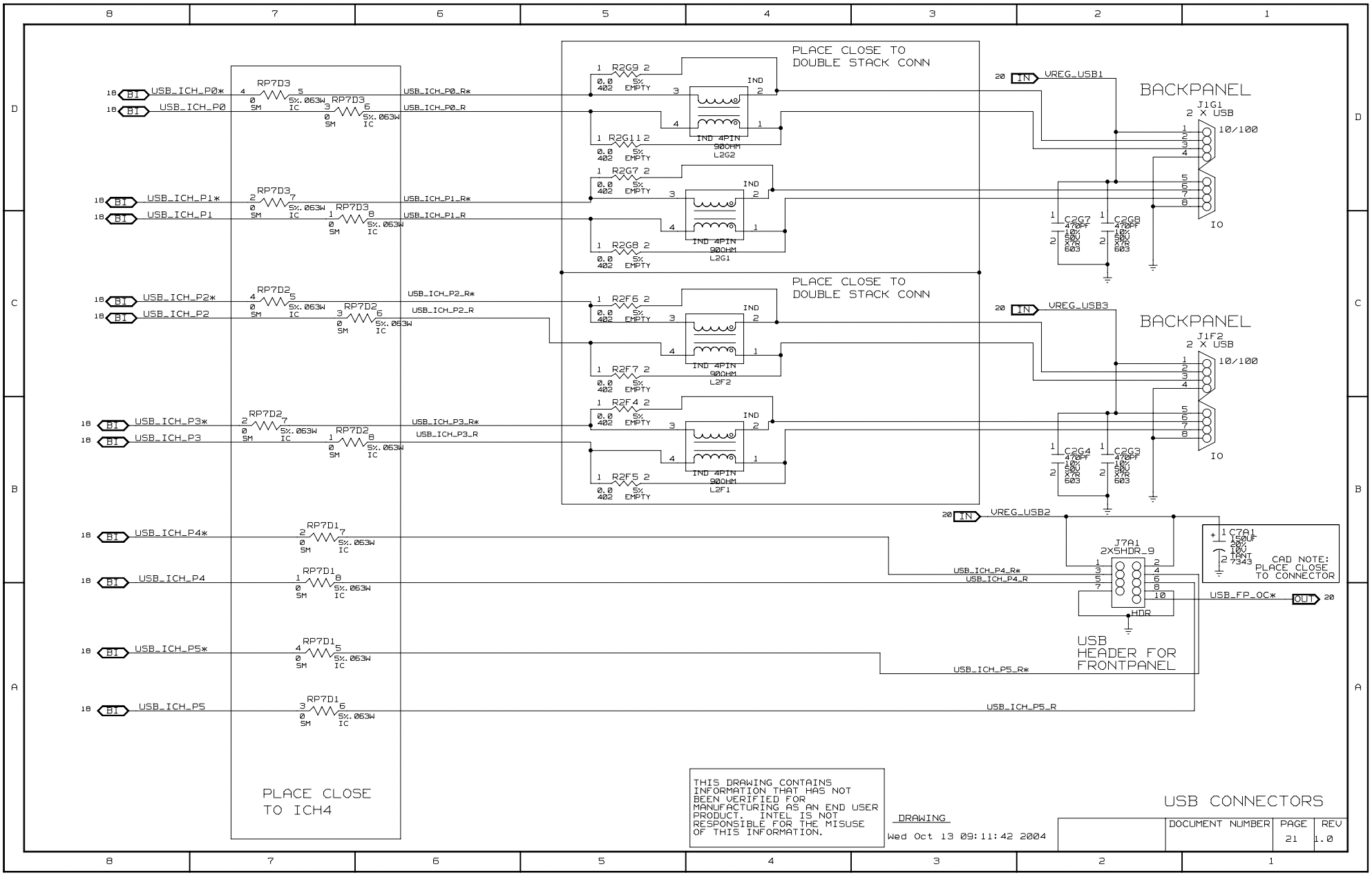
USB WAKE POWER

DOCUMENT NUMBER	PAGE	REV
	20	1.0


PLACE CLOSE TO DOUBLE STACK CONN
PLACE CLOSE TO DOUBLE STACK CONN
BACKPANEL
J1G1
2 X USB
10/100
IO
BACKPANEL
J1F2
2 X USB
10/100
IO
VREG_USB1
VREG_USB3
VREG_USB2
USB_ICH_P0*
USB_ICH_P0
USB_ICH_P1*
USB_ICH_P1
USB_ICH_P2*
USB_ICH_P2
USB_ICH_P3*
USB_ICH_P3
USB_ICH_P4*
USB_ICH_P4
USB_ICH_P5*
USB_ICH_P5
USB_FP_OC*
J7A1
2X5HDR_9
HDR
USB HEADER FOR FRONTPANEL
CAD NOTE: PLACE CLOSE TO CONNECTOR
PLACE CLOSE TO ICH4
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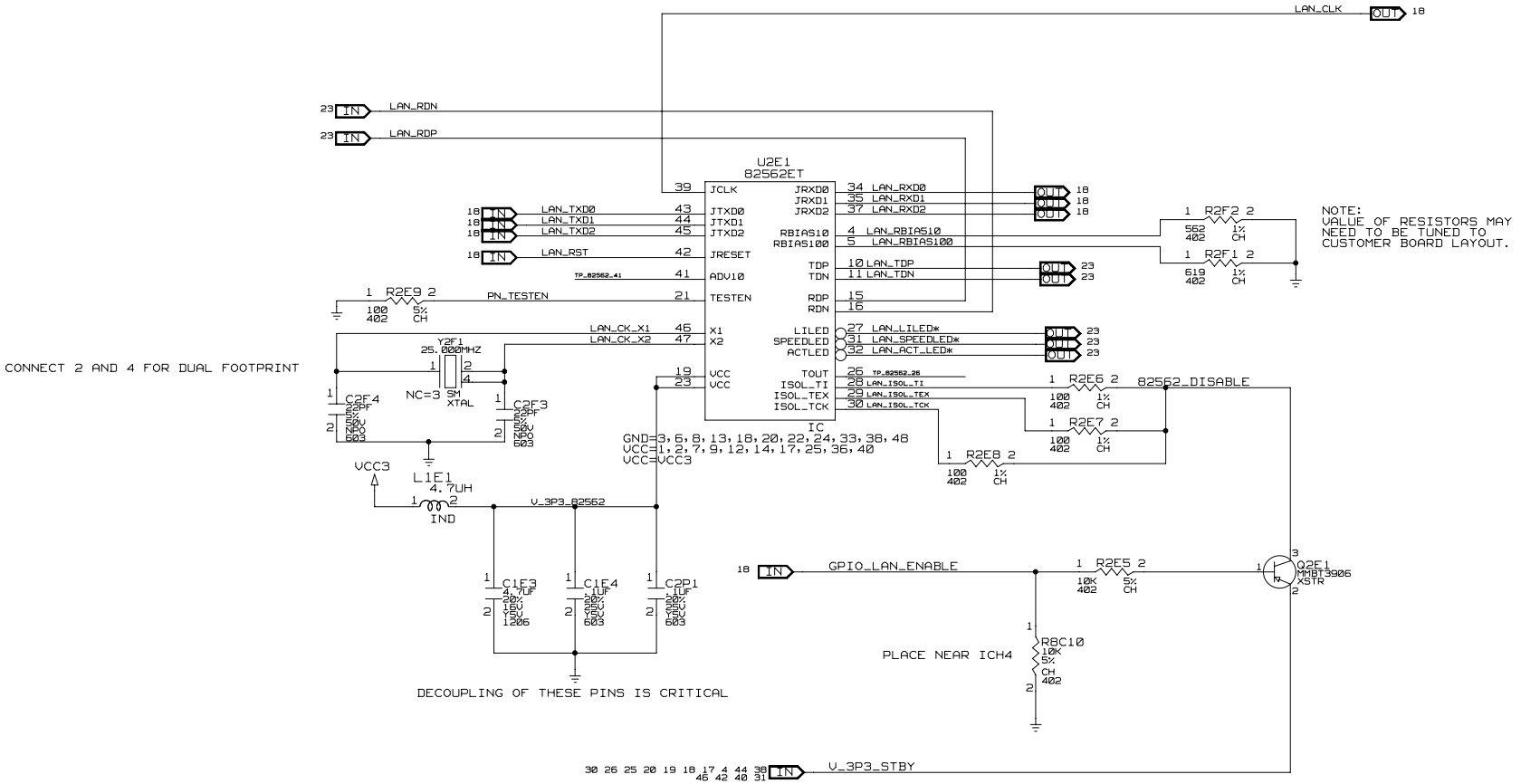
DRAWING
Wed Oct 13 09:11:42 2004
USB CONNECTORS
DOCUMENT NUMBER
PAGE
21
REV
1.0



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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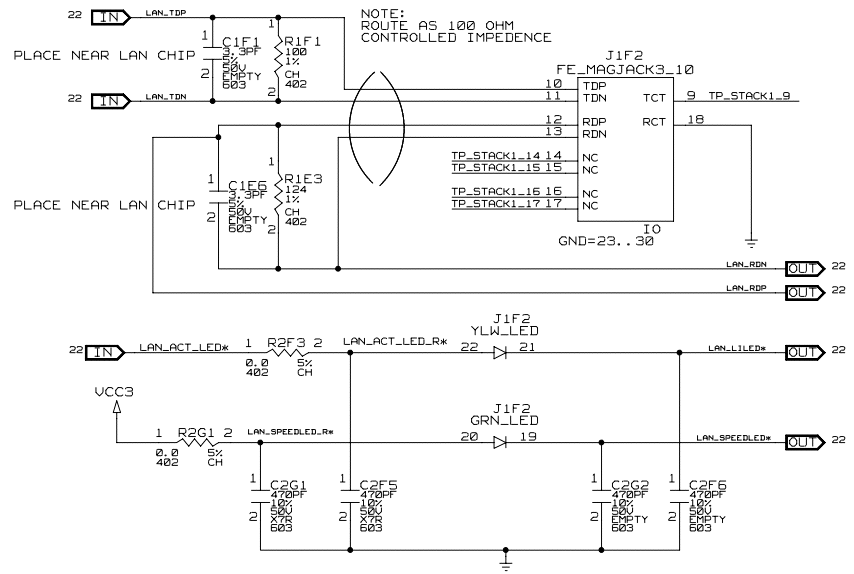
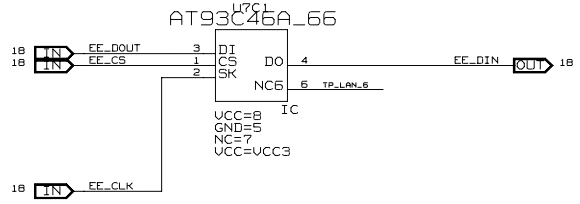
82562 ETHERNET PHY

	DOCUMENT NUMBER	PAGE	REV
		22	1.0

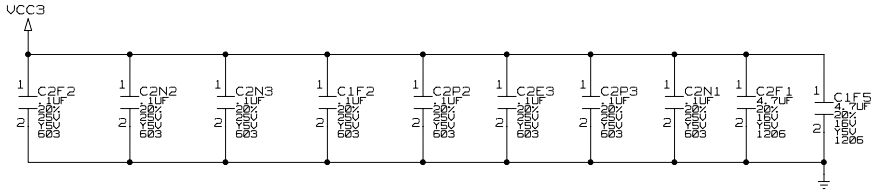
SP_JACK



LAN E2 PROM



LAN DECOUPLING



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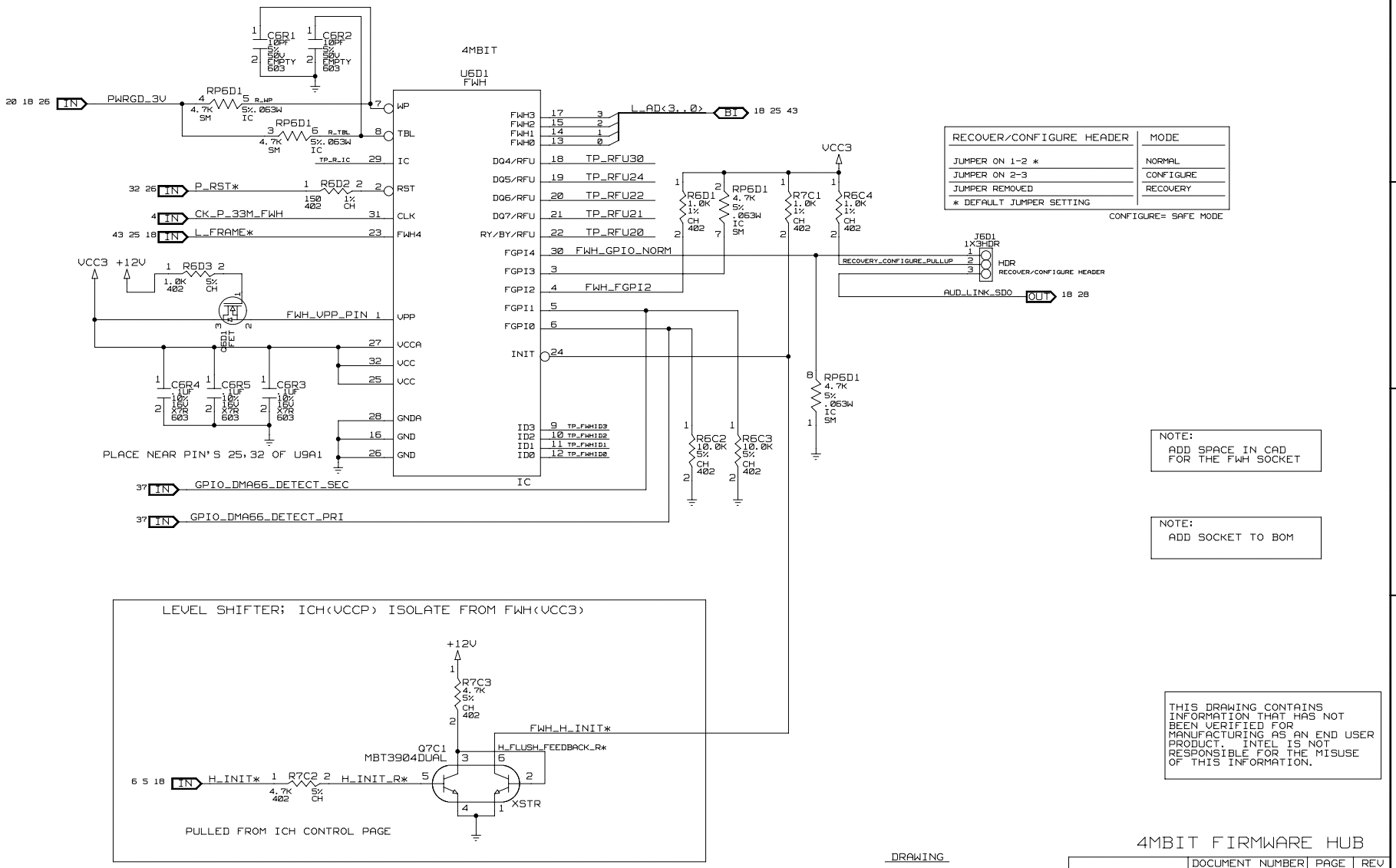
Wed Oct 13 09:11:43 2004

LAN CONNECTOR / MISC

DOCUMENT NUMBER	PAGE	REV
	23	1.0


4MBIT
U6D1
FWH
C6R1
C6R2
RP6D1
PWRGD_3V
WP
TBL
IC
RST
CLK
FWH4
VPP
VCCA
VCC
GNDA
GND
P_RST*
CK_P_33M_FWH
L_FRAME*
FWH_VPP_PIN
PLACE NEAR PIN'S 25,32 OF U9A1
GPIO_DMA66_DETECT_SEC
GPIO_DMA66_DETECT_PRI
L_AD<3..0>
FWH_GPIO_NORM
FWH_FGPI2
TP_RFU30
TP_RFU24
TP_RFU22
TP_RFU21
TP_RFU20
R6D1
R7C1
R6C4
R6C2
R6C3
J6D1
HDR
RECOVER/CONFIGURE HEADER
RECOVERY_CONFIGURE_PULLUP
AUD_LINK_SDO
RECOVER/CONFIGURE HEADER | MODE
JUMPER ON 1-2 * | NORMAL
JUMPER ON 2-3 | CONFIGURE
JUMPER REMOVED | RECOVERY
* DEFAULT JUMPER SETTING
CONFIGURE= SAFE MODE
NOTE: ADD SPACE IN CAD FOR THE FWH SOCKET
NOTE: ADD SOCKET TO BOM
LEVEL SHIFTER; ICH(VCCP) ISOLATE FROM FWH(VCC3)
+12V
R7C3
Q7C1
MBT3904DUAL
FWH_H_INIT*
H_FLUSH_FEEDBACK_R*
H_INIT*
H_INIT_R*
R7C2
XSTR
PULLED FROM ICH CONTROL PAGE
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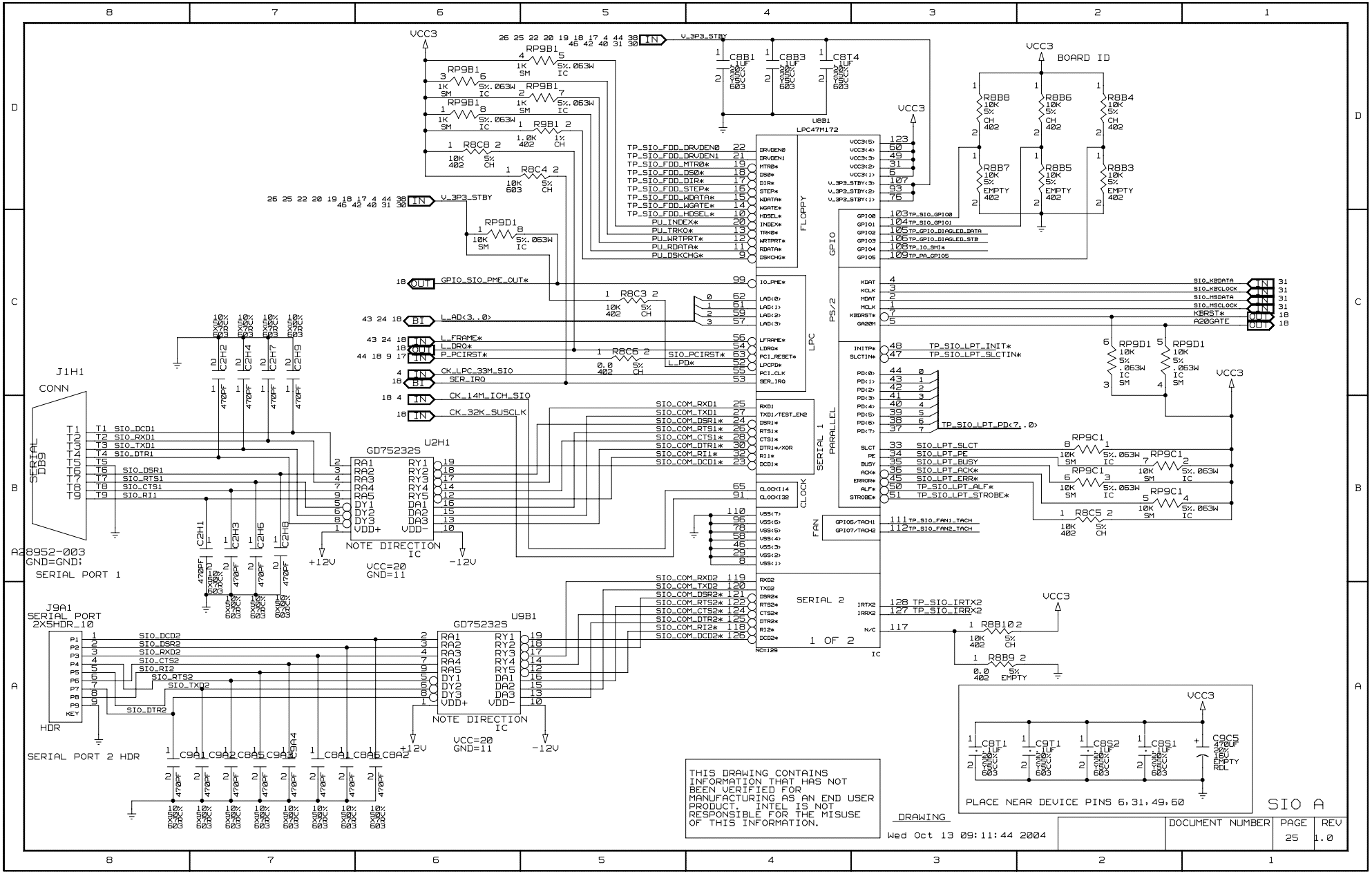
DRAWING
Wed Oct 13 09:11:43 2004
4MBIT FIRMWARE HUB
DOCUMENT NUMBER
PAGE 24
REV 1.0


SIO A
BOARD ID
U8B1
LPC47M172
U2H1
GD75232S
U9B1
J1H1
CONN
SERIAL PORT 1
A28952-003
GND=GND;
J9A1
SERIAL PORT 2X5HDR_10
HDR
SERIAL PORT 2 HDR
NOTE DIRECTION IC
VCC=20
GND=11
+12V
-12V
SERIAL 2
1 OF 2
FLOPPY
GPIO
PS/2
LPC
SERIAL 1
PARALLEL
CLOCK
FAN
PLACE NEAR DEVICE PINS 6,31,49,60
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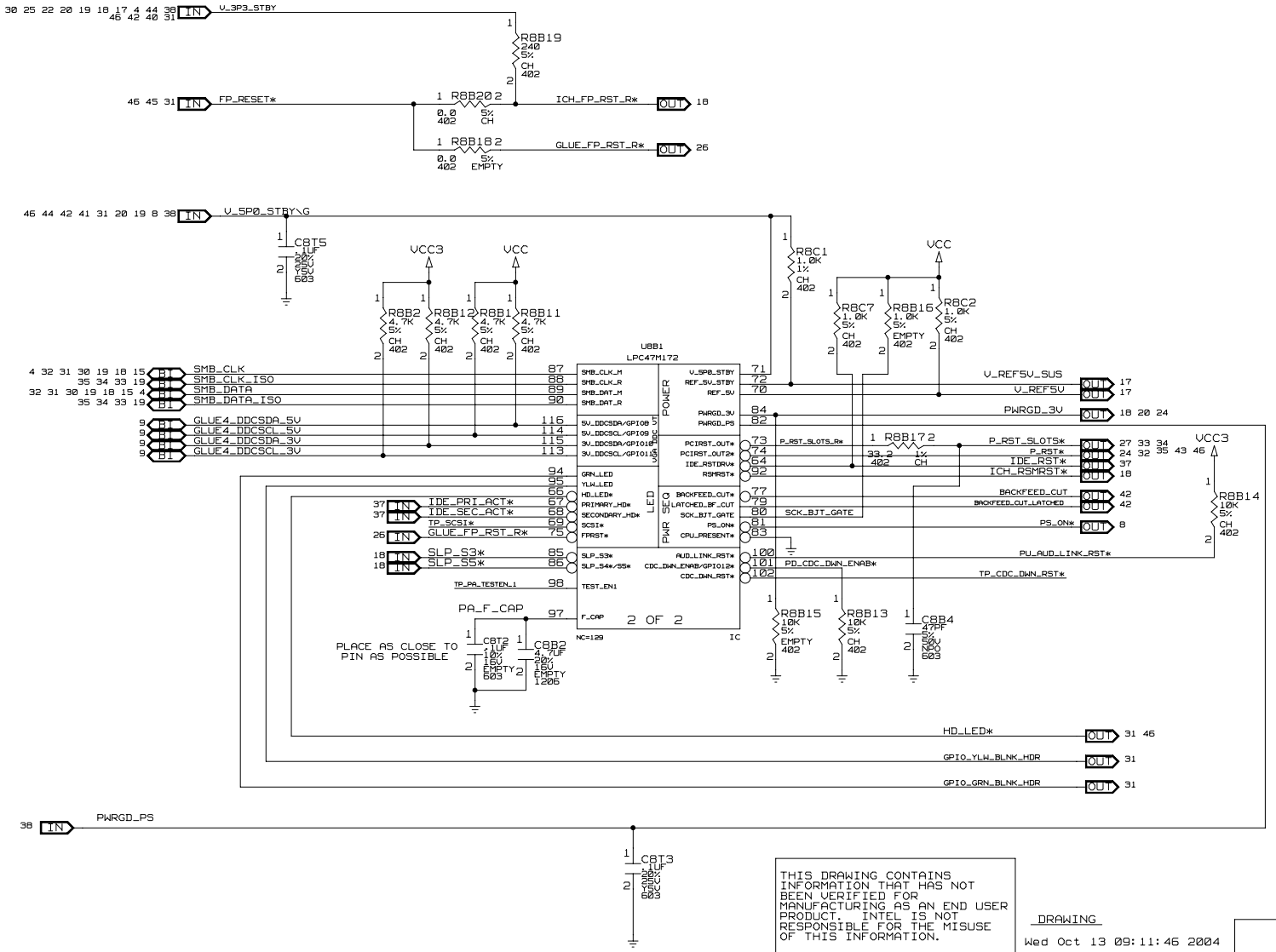
DRAWING
Wed Oct 13 09:11:44 2004
DOCUMENT NUMBER
PAGE 25
REV 1.0


V_3P3_STBY
R8B19
240
FP_RESET*
R8B202
0.0
ICH_FP_RST_R*
R8B182
GLUE_FP_RST_R*
V_5P0_STBY\G
C8T5
.1UF
R8B2
R8B12
R8B1
R8B11
4.7K
VCC3
VCC
R8C1
1.0K
R8C7
R8B16
R8C2
UBB1
LPC47M172
SMB_CLK
SMB_CLK_ISO
SMB_DATA
SMB_DATA_ISO
GLUE4_DDCSDA_5V
GLUE4_DDCSCL_5V
GLUE4_DDCSDA_3V
GLUE4_DDCSCL_3V
V_5P0_STBY
REF_5V_STBY
REF_5V
PWRGD_3V
PWRGD_PS
PCIRST_OUT*
IDE_RSTDRV*
RSMRST*
BACKFEED_OUT*
LATCHED_BF_OUT
SCK_BJT_GATE
PS_ON*
CPU_PRESENT*
AUD_LINK_RST*
CDC_DWN_ENAB/GPIO12*
CDC_DWN_RST*
GRN_LED
YLW_LED
HD_LED*
PRIMARY_HD*
SECONDARY_HD*
SCSI*
FPRST*
SLP_S3*
SLP_S4#/S5*
TEST_EN1
F_CAP
2 OF 2
NC=129
IC
V_REF5V_SUS
V_REF5V
PWRGD_3V
P_RST_SLOTS*
P_RST*
IDE_RST*
ICH_RSMRST*
BACKFEED_OUT
BACKFEED_OUT_LATCHED
PS_ON*
PU_AUD_LINK_RST*
PD_CDC_DWN_ENABLE*
TP_CDC_DWN_RST*
R8B172
33.2
R8B14
10K
R8B15
R8B13
C8B4
47PF
IDE_PRI_ACT*
IDE_SEC_ACT*
TP_SCSI*
GLUE_FP_RST_R*
SLP_S3*
SLP_S5*
TP_PA_TESTEN_1
PA_F_CAP
C8T2
C8B2
4.7UF
PLACE AS CLOSE TO PIN AS POSSIBLE
HD_LED*
GPIO_YLW_BLNK_HDR
GPIO_GRN_BLNK_HDR
PWRGD_PS
C8T3
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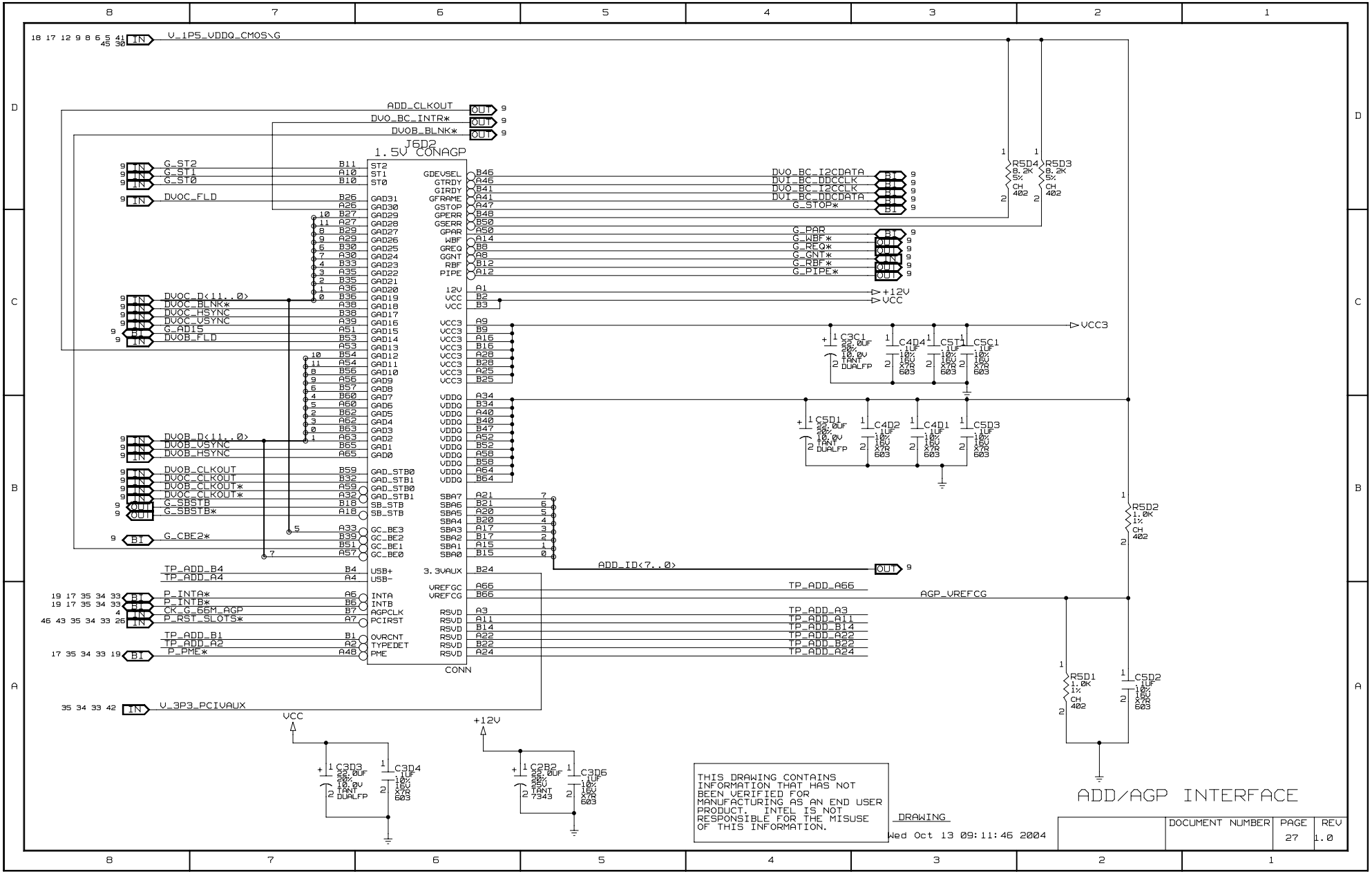
DRAWING
Wed Oct 13 09:11:45 2004
SIO B
DOCUMENT NUMBER
PAGE
26
REV
1.0


V_1P5_VDDQ_CMOS\G
ADD_CLKOUT
DVO_BC_INTR*
DVOB_BLNK*
J6D2
1.5V CONAGP
G_ST2
G_ST1
G_ST0
DVOC_FLD
DVOC_D<11..0>
DVOC_BLNK*
DVOC_HSYNC
DVOC_VSYNC
G_ADI5
DVOB_FLD
DVOB_D<11..0>
DVOB_VSYNC
DVOB_HSYNC
DVOB_CLKOUT
DVOC_CLKOUT
DVOB_CLKOUT*
DVOC_CLKOUT*
G_SBSTB
G_SBSTB*
G_CBE2*
TP_ADD_B4
TP_ADD_A4
P_INTA*
P_INTB*
CK_G_66M_AGP
P_RST_SLOTS*
TP_ADD_B1
TP_ADD_A2
P_PME*
V_3P3_PCIVAUX
CONN
DVO_BC_I2CDATA
DVI_BC_DDCCLK
DVO_BC_I2CCLK
DVI_BC_DDCDATA
G_STOP*
G_PAR
G_WBF*
G_REQ*
G_GNT*
G_RBF*
G_PIPE*
+12V
VCC
VCC3
ADD_ID<7..0>
TP_ADD_A66
AGP_VREFCG
TP_ADD_A3
TP_ADD_A11
TP_ADD_B14
TP_ADD_A22
TP_ADD_B22
TP_ADD_A24
R5D4 8.2K 5% CH 402
R5D3 8.2K 5% CH 402
R5D2 1.0K 1% CH 402
R5D1 1.0K 1% CH 402
C3C1 22.0UF 20% 10.0V TANT DUALFP
C4D4 .1UF 10% 16V X7R 603
C5T1 .1UF 10% 16V X7R 603
C5C1 .1UF 10% 16V X7R 603
C5D1 22.0UF 20% 10.0V TANT DUALFP
C4D2 .1UF 10% 16V X7R 603
C4D1 .1UF 10% 16V X7R 603
C5D3 .1UF 10% 16V X7R 603
C5D2 .1UF 10% 16V X7R 603
C3D3 22.0UF 20% 10.0V TANT DUALFP
C3D4 .1UF 10% 16V X7R 603
C2B2 22.0UF 20% 25V TANT 7343
C3D6 .1UF 10% 16V X7R 603
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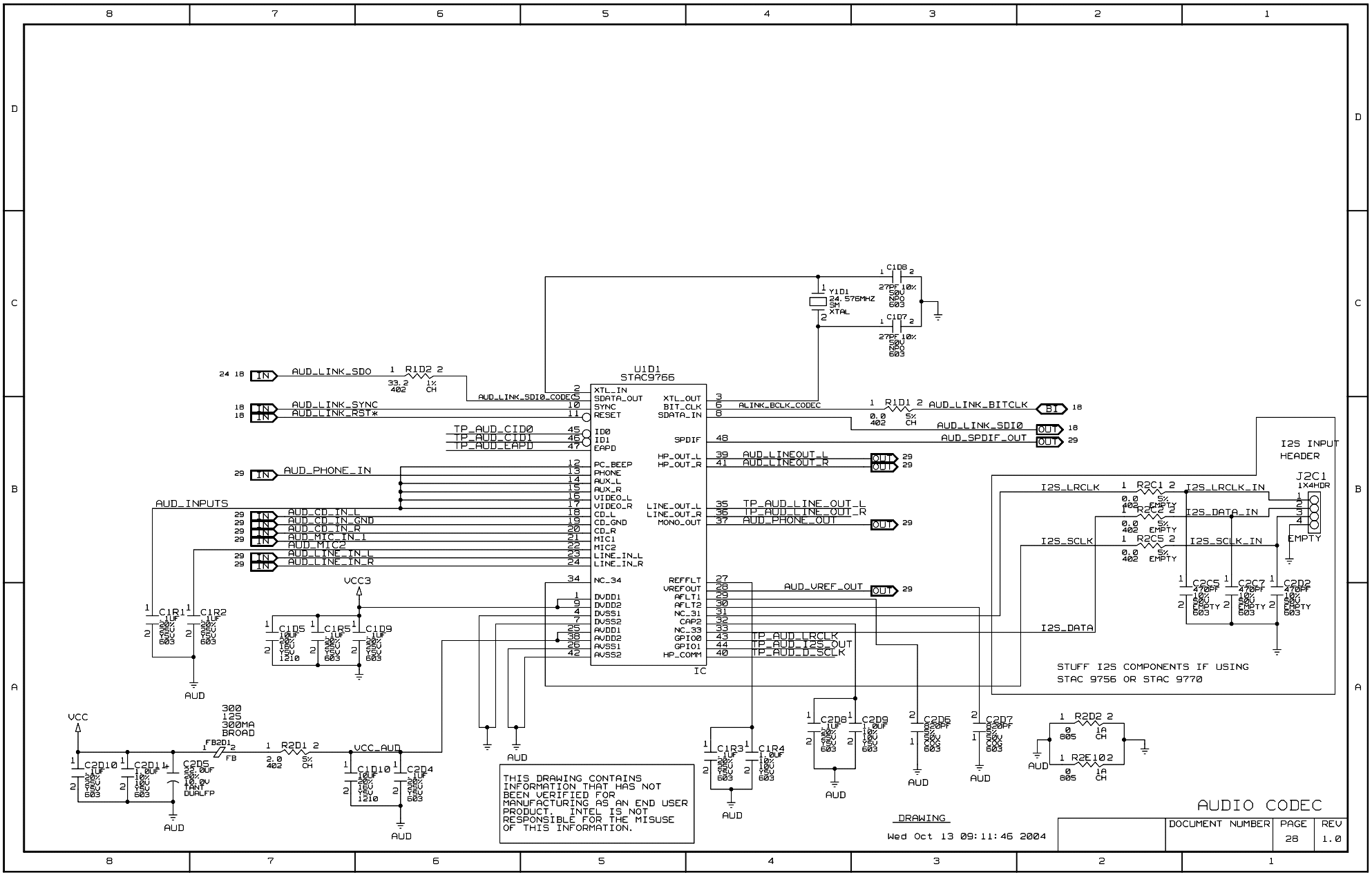
DRAWING
Wed Oct 13 09:11:45 2004
ADD/AGP INTERFACE
DOCUMENT NUMBER
PAGE 27
REV 1.0


U1D1
STAC9766
XTL_IN
SDATA_OUT
SYNC
RESET
ID0
ID1
EAPD
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
NC_34
DVDD1
DVDD2
DVSS1
DVSS2
AVDD1
AVDD2
AVSS1
AVSS2
XTL_OUT
BIT_CLK
SDATA_IN
SPDIF
HP_OUT_L
HP_OUT_R
LINE_OUT_L
LINE_OUT_R
MONO_OUT
REFFLT
VREFOUT
AFLT1
AFLT2
NC_31
CAP2
NC_33
GPIO0
GPIO1
HP_COMM
IC
AUD_LINK_SDO
AUD_LINK_SDI0_CODEC
AUD_LINK_SYNC
AUD_LINK_RST*
TP_AUD_CID0
TP_AUD_CID1
TP_AUD_EAPD
AUD_PHONE_IN
AUD_INPUTS
AUD_CD_IN_L
AUD_CD_IN_GND
AUD_CD_IN_R
AUD_MIC_IN_1
AUD_MIC2
AUD_LINE_IN_L
AUD_LINE_IN_R
ALINK_BCLK_CODEC
AUD_LINK_BITCLK
AUD_LINK_SDI0
AUD_SPDIF_OUT
AUD_LINEOUT_L
AUD_LINEOUT_R
TP_AUD_LINE_OUT_L
TP_AUD_LINE_OUT_R
AUD_PHONE_OUT
AUD_VREF_OUT
TP_AUD_LRCLK
TP_AUD_I2S_OUT
TP_AUD_D_SCLK
Y1D1
24.576MHZ
XTAL
VCC
VCC3
VCC_AUD
AUD
I2S INPUT
HEADER
J2C1
I2S_LRCLK
I2S_SCLK
I2S_DATA
I2S_LRCLK_IN
I2S_DATA_IN
I2S_SCLK_IN
STUFF I2S COMPONENTS IF USING
STAC 9756 OR STAC 9770
THIS DRAWING CONTAINS
INFORMATION THAT HAS NOT
BEEN VERIFIED FOR
MANUFACTURING AS AN END USER
PRODUCT. INTEL IS NOT
RESPONSIBLE FOR THE MISUSE
OF THIS INFORMATION.
DRAWING
Wed Oct 13 09:11:45 2004
AUDIO CODEC
DOCUMENT NUMBER
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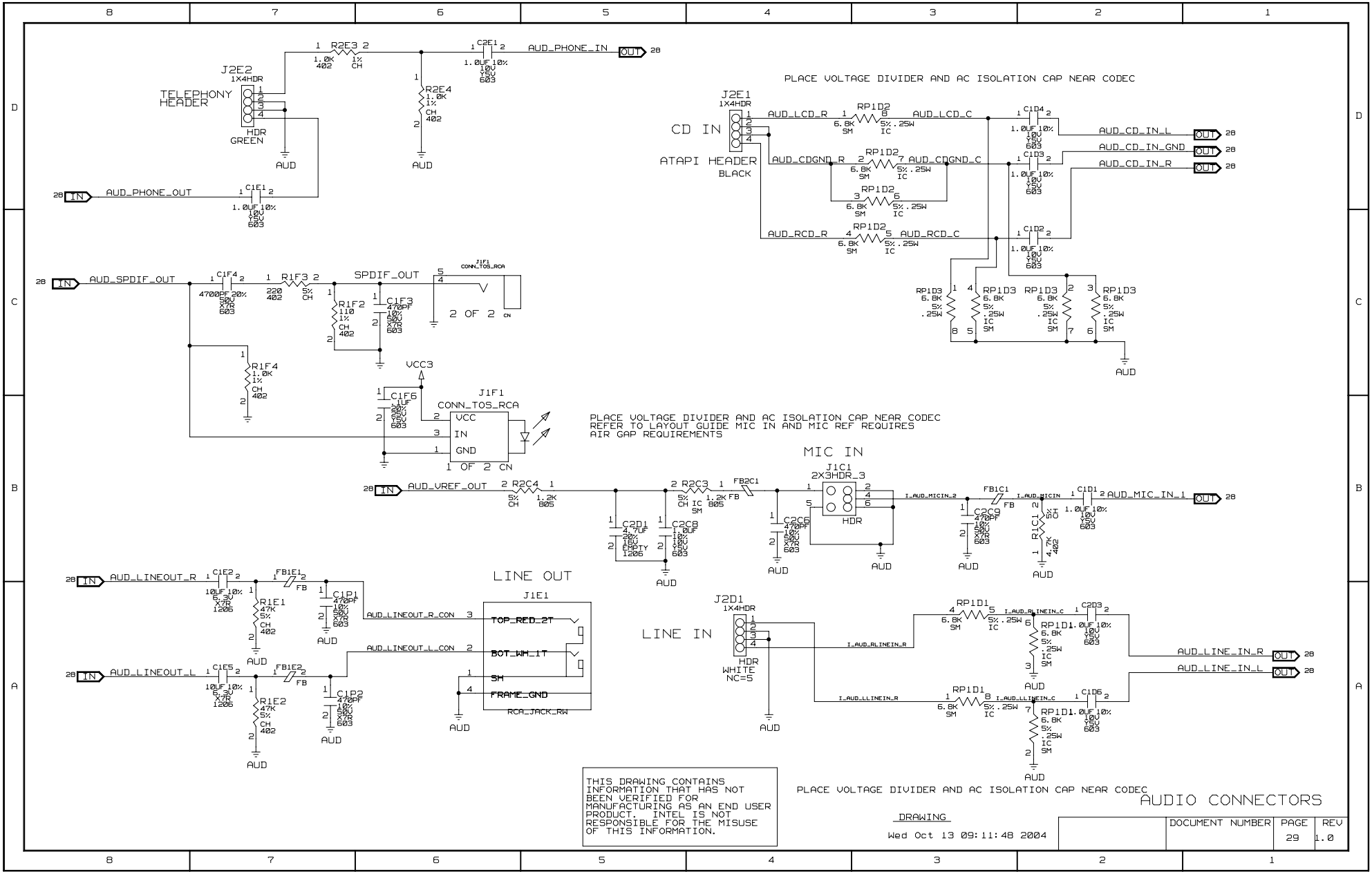
28
REV
1.0


J2E2
1X4HDR
TELEPHONY HEADER
HDR
GREEN
R2E3
1.0K
402
1%
CH
C2E1
1.0UF 10%
10V
Y5V
603
R2E4
1.0K
1%
CH
402
AUD_PHONE_IN
OUT 28
AUD
C1E1
AUD_PHONE_OUT
IN 28
PLACE VOLTAGE DIVIDER AND AC ISOLATION CAP NEAR CODEC
J2E1
1X4HDR
CD IN
ATAPI HEADER
BLACK
AUD_LCD_R
AUD_LCD_C
AUD_CDGND_R
AUD_CDGND_C
AUD_RCD_R
AUD_RCD_C
RP1D2
6.8K
SM
5% .25W
IC
C1D4
C1D3
C1D2
AUD_CD_IN_L
AUD_CD_IN_GND
AUD_CD_IN_R
RP1D3
6.8K
5%
.25W
IC
SM
AUD_SPDIF_OUT
C1F4
4700PF 20%
50V
X7R
603
R1F3
220
402
5%
CH
SPDIF_OUT
J1F1
CONN_TOS_RCA
2 OF 2 CN
R1F2
110
1%
CH
402
C1F3
470PF
10%
50V
X7R
603
R1F4
1.0K
1%
CH
402
VCC3
C1F6
1UF
80%
25V
Y5V
603
VCC
IN
GND
1 OF 2 CN
PLACE VOLTAGE DIVIDER AND AC ISOLATION CAP NEAR CODEC
REFER TO LAYOUT GUIDE MIC IN AND MIC REF REQUIRES
AIR GAP REQUIREMENTS
MIC IN
J1C1
2X3HDR_3
HDR
AUD_VREF_OUT
R2C4
1.2K
805
R2C3
FB2C1
C2D1
4.7UF
20%
10V
TANTY
1206
C2C8
1.0UF
10%
10V
Y5V
603
C2C9
470PF
10%
50V
X7R
603
FB1C1
I_AUD_MICIN_2
I_AUD_MICIN
R1C1
10
1%
4.7K
402
AUD_MIC_IN_1
LINE OUT
J1E1
TOP_RED_2T
BOT_WH_1T
SH
FRAME_GND
RCA_JACK_RW
AUD_LINEOUT_R
AUD_LINEOUT_L
AUD_LINEOUT_R_CON
AUD_LINEOUT_L_CON
C1E2
C1E5
10UF 10%
6.3V
X7R
1206
FB1E1
FB1E2
FB
R1E1
47K
5%
CH
402
R1E2
C1P1
C1P2
470PF
10%
50V
X7R
603
LINE IN
J2D1
1X4HDR
HDR
WHITE
NC=5
I_AUD_RLINEIN_R
I_AUD_LLINEIN_R
I_AUD_RLINEIN_C
I_AUD_LLINEIN_C
RP1D1
C2D3
C1D5
AUD_LINE_IN_R
AUD_LINE_IN_L
PLACE VOLTAGE DIVIDER AND AC ISOLATION CAP NEAR CODEC
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
AUDIO CONNECTORS
DRAWING
Wed Oct 13 09:11:48 2004
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PAGE
29
REV
1.0

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP
PLACE THERMAL TRANSISTOR BY PCI CONNECTOR

NOTE:
PLACE HECETA6
BY THE PROCESSOR

PRELIMINARY
U7H1
HECETA6

PLACE ACCORDING TO SYSTEM THERMAL DESIGN ENGINEER DIRECTION

IC

FAN 1

CPU

FAN 2

CHASSIS
REAR - BY IO

FAN 3

CHASSIS
FRONT - BY FP

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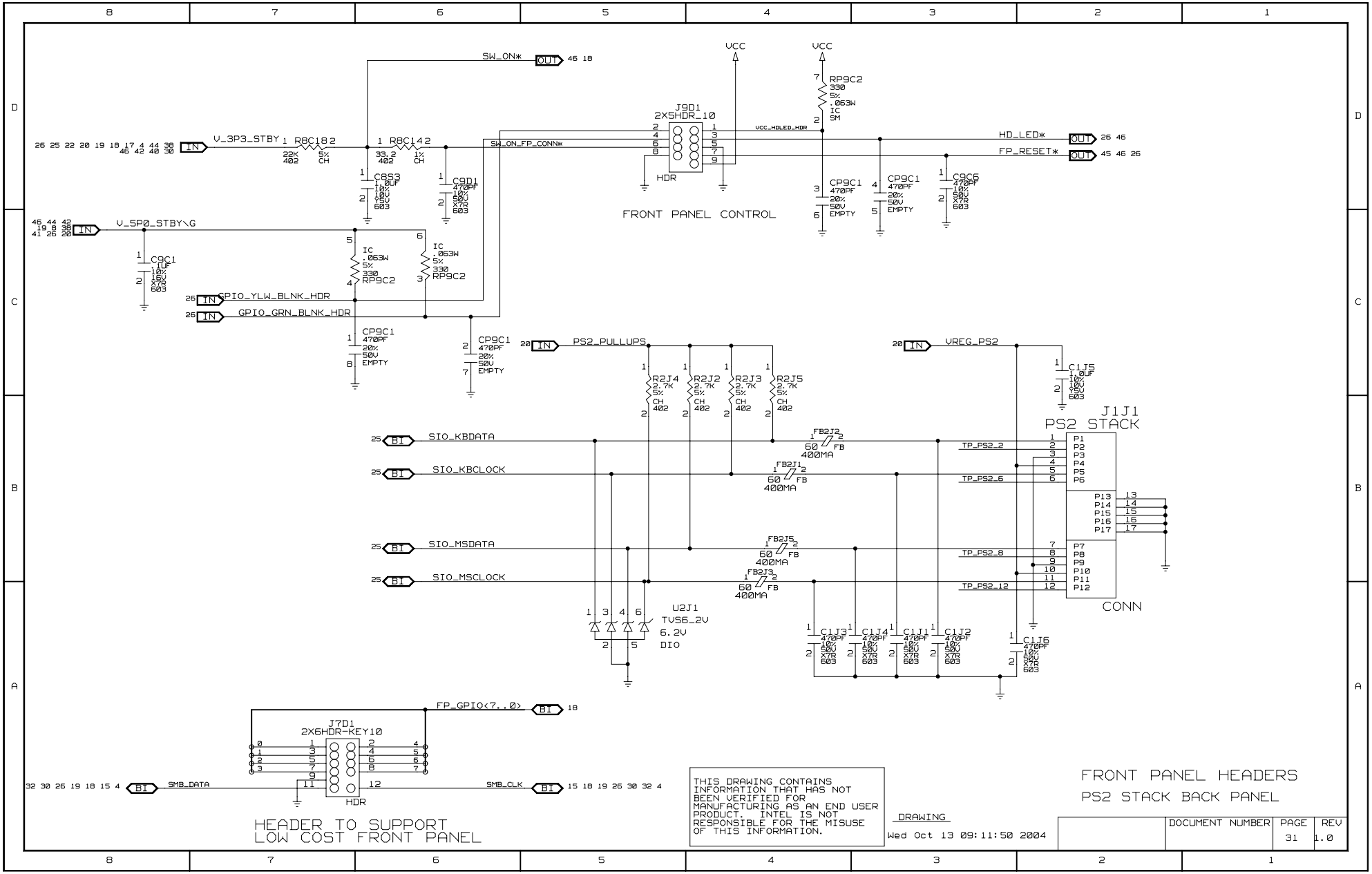
SYS MONITOR / FAN CONTROL

DRAWING
Wed Oct 13 09:11:49 2004

DOCUMENT NUMBER	PAGE	REV
	30	1.0


SW_ON*
OUT 46 18
VCC
VCC
RP9C2
330
5%
.063W
IC
SM
J9D1
2X5HDR_10
HDR
VCC_HDLED_HDR
HD_LED*
OUT 26 46
FP_RESET*
OUT 45 46 26
FRONT PANEL CONTROL
26 25 22 20 19 18 17 4 44 38 46 42 40 30
IN
V_3P3_STBY
R8C18
22K
5%
CH
402
R8C14
33.2
1%
CH
402
SW_ON_FP_CONN*
C8S3
1.0UF
10%
10V
Y5V
603
C9D1
470PF
10%
50V
X7R
603
CP9C1
470PF
20%
50V
EMPTY
C9C6
470PF
10%
50V
X7R
603
46 44 42 38 19 8 41 26 20
IN
V_5P0_STBY\G
C9C1
1UF
10%
10V
X7R
603
IC
.063W
5%
330
RP9C2
GPIO_YLW_BLNK_HDR
GPIO_GRN_BLNK_HDR
20
IN
PS2_PULLUPS
VREG_PS2
R2J4
R2J2
R2J3
R2J5
2.7K
5%
CH
402
C1J5
1.0UF
10%
10V
Y5V
603
J1J1
PS2 STACK
CONN
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
25
BI
SIO_KBDATA
SIO_KBCLOCK
SIO_MSDATA
SIO_MSCLOCK
FB2J2
FB2J1
FB2J5
FB2J3
60
400MA
FB
TP_PS2_2
TP_PS2_6
TP_PS2_8
TP_PS2_12
U2J1
TVS6_2V
6.2V
DIO
C1J3
C1J4
C1J1
C1J2
C1J6
470PF
10%
50V
X7R
603
FP_GPIO<7..0>
18
J7D1
2X6HDR-KEY10
HDR
32 30 26 19 18 15 4
SMB_DATA
SMB_CLK
15 18 19 26 30 32 4
HEADER TO SUPPORT
LOW COST FRONT PANEL
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INFORMATION THAT HAS NOT
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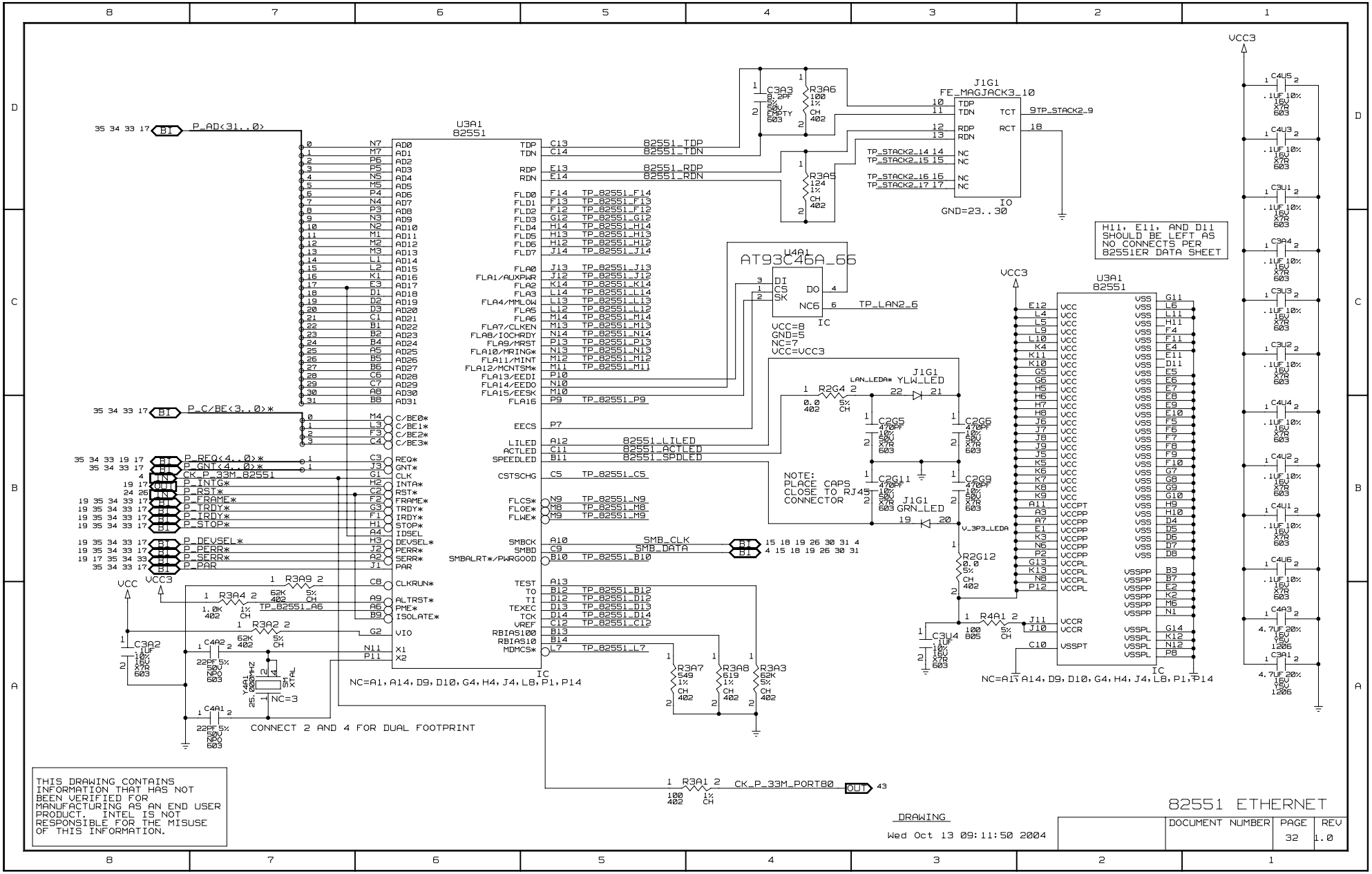
FRONT PANEL HEADERS
PS2 STACK BACK PANEL
DOCUMENT NUMBER
PAGE
31
REV
1.0


U3A1
82551
P_AD<31..0>
P_C/BE<3..0>*
P_REQ<4..0>*
P_GNT<4..0>*
CK_P_33M_82551
P_INTG*
P_RST*
P_FRAME*
P_TRDY*
P_IRDY*
P_STOP*
P_DEVSEL*
P_PERR*
P_SERR*
P_PAR
CLKRUN*
ALTRST*
PME*
ISOLATE*
VIO
X1
X2
TDP
TDN
RDP
RDN
FLD0
FLD1
FLD2
FLD3
FLD4
FLD5
FLD6
FLD7
FLA0
FLA1/AUXPWR
FLA2
FLA3
FLA4/MMLOW
FLA5
FLA6
FLA7/CLKEN
FLA8/IOCHRDY
FLA9/MRST
FLA10/MRING*
FLA11/MINT
FLA12/MCNTSM*
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16
EECS
LILED
ACTLED
SPEEDLED
CSTSCHG
FLCS*
FLOE*
FLWE*
SMBCK
SMBD
SMBALRT*/PWRGOOD
TEST
TO
TI
TEXEC
TCK
VREF
RBIAS100
RBIAS10
MDMCS*
82551_TDP
82551_TDN
82551_RDP
82551_RDN
82551_LILED
82551_ACTLED
82551_SPDLED
SMB_CLK
SMB_DATA
IC
NC=A1, A14, D9, D10, G4, H4, J4, L8, P1, P14
CONNECT 2 AND 4 FOR DUAL FOOTPRINT
J1G1
FE_MAGJACK3_10
TDP
TDN
RDP
RDN
TCT
RCT
NC
IO
GND=23..30
U4A1
AT93C46A_66
DI
CS
SK
DO
NC6
TP_LAN2_6
VCC=8
GND=5
NC=7
VCC=VCC3
LAN_LEDA*
YLW_LED
GRN_LED
V_3P3_LEDA
NOTE:
PLACE CAPS
CLOSE TO RJ45
CONNECTOR
H11, E11, AND D11
SHOULD BE LEFT AS
NO CONNECTS PER
82551ER DATA SHEET
VCC3
VCC
VCCPT
VCCPP
VCCPL
VSS
VSSPP
VSSPL
VSSPT
CK_P_33M_PORT80
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INFORMATION THAT HAS NOT
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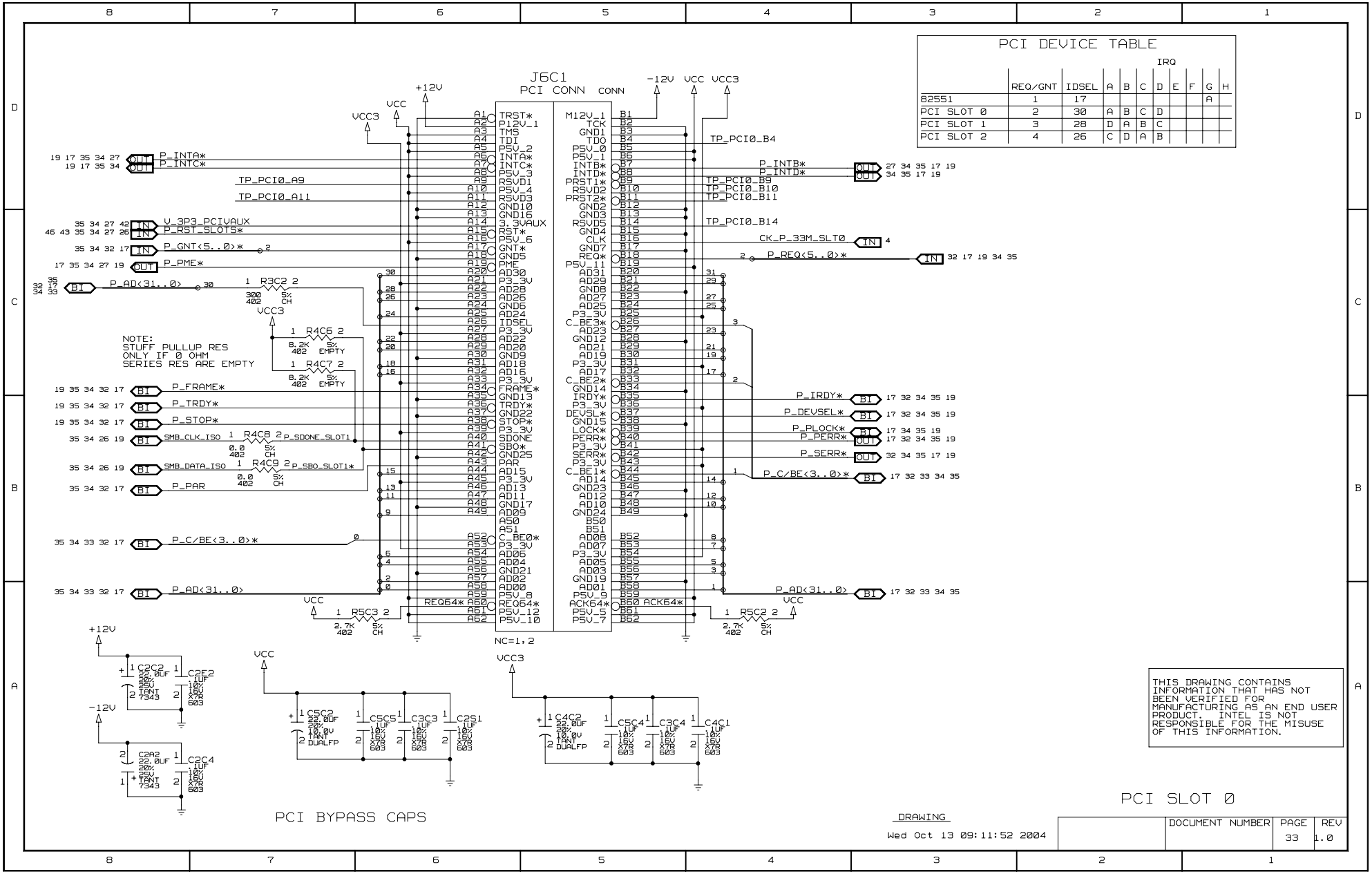
DRAWING
Wed Oct 13 09:11:50 2004
82551 ETHERNET
DOCUMENT NUMBER
PAGE
32
REV
1.0



PCI DEVICE TABLE

	REQ/GNT	IDSEL	IRQ A	B	C	D	E	F	G	H
82551	1	17							A	
PCI SLOT 0	2	30	A	B	C	D				
PCI SLOT 1	3	28	D	A	B	C				
PCI SLOT 2	4	26	C	D	A	B				

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PCI SLOT 0

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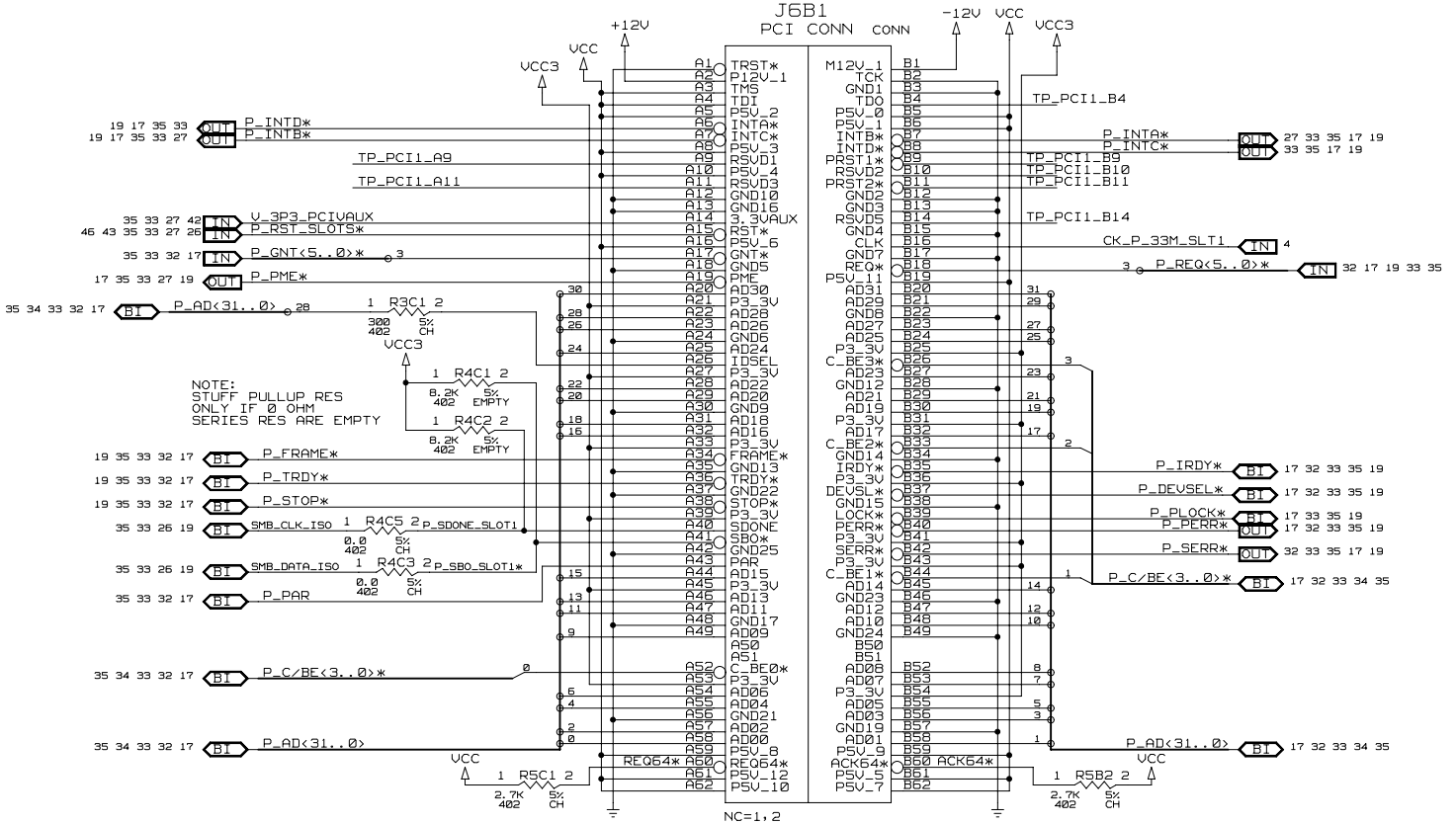
Wed Oct 13 09:11:52 2004

DOCUMENT NUMBER	PAGE	REV
	33	1.0



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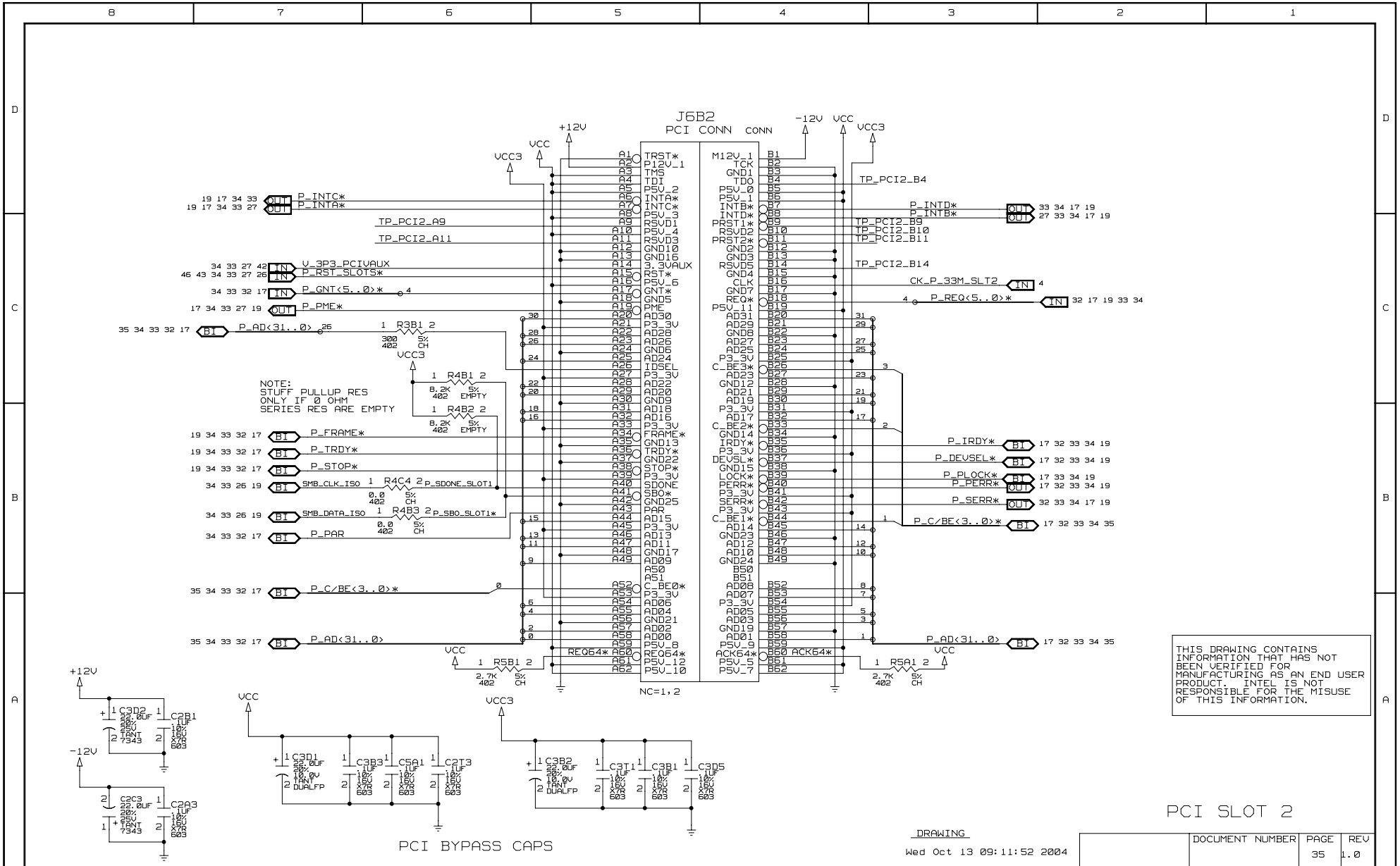
PCI SLOT 1

DRAWING
Wed Oct 13 09:11:52 2004

DOCUMENT NUMBER	PAGE	REV
	34	1.0



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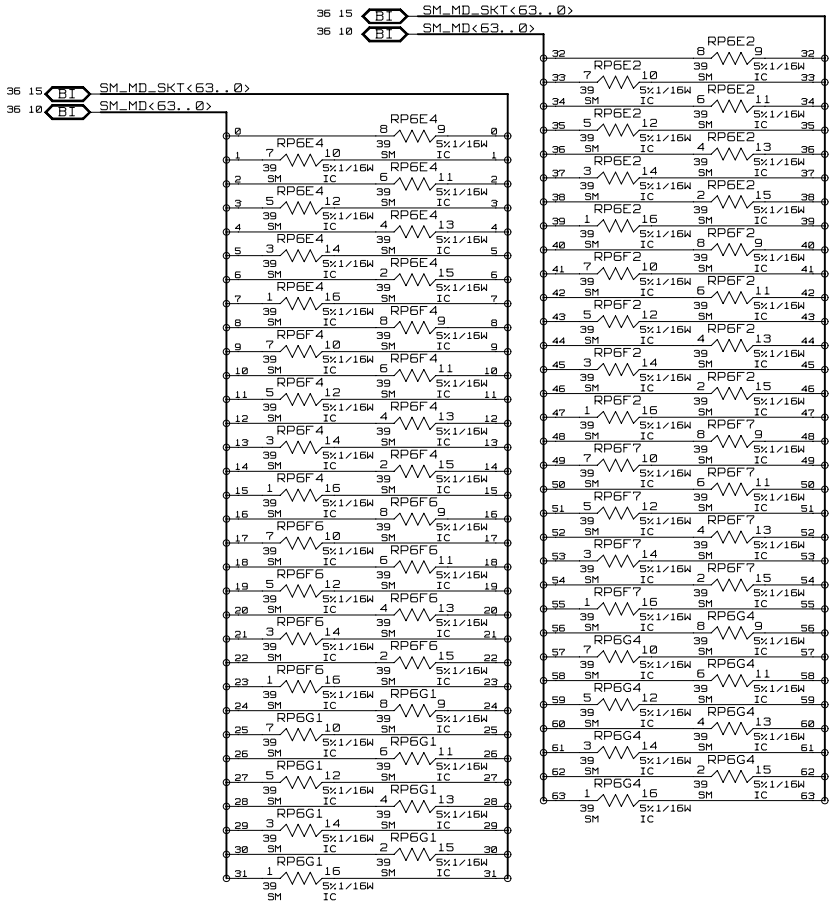
PCI SLOT 2

DRAWING

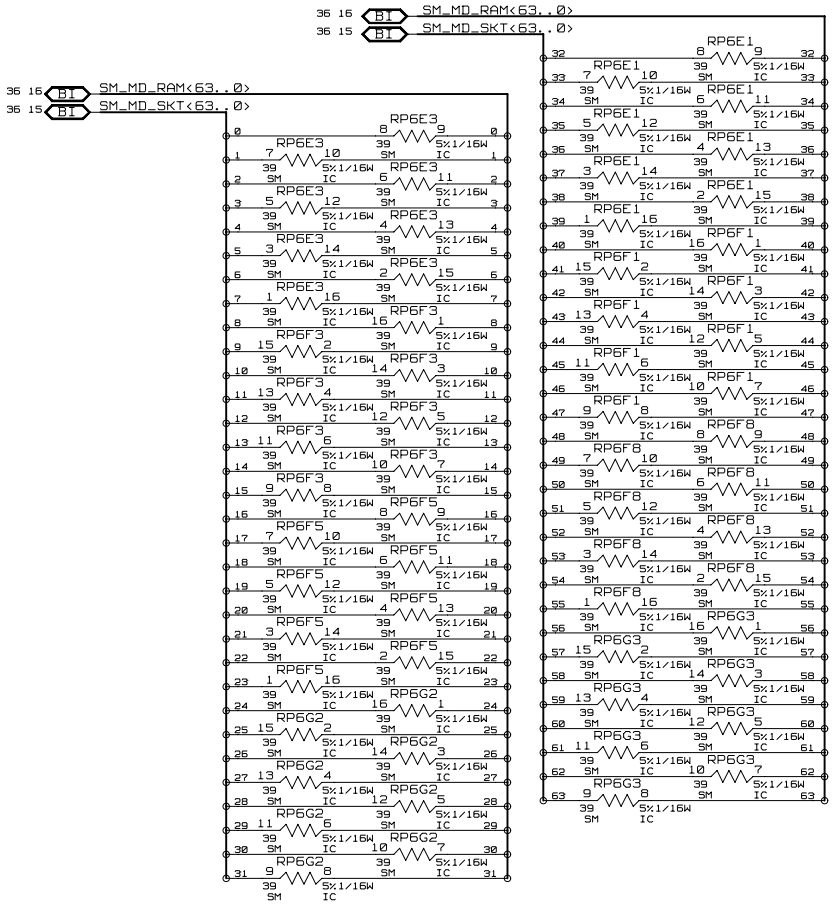
Wed Oct 13 09:11:52 2004

	DOCUMENT NUMBER	PAGE	REV
		35	1.0

PLACE R-PACK CLOSE TO SOCKET



PLACE R-PACKS CLOSE TO RAM



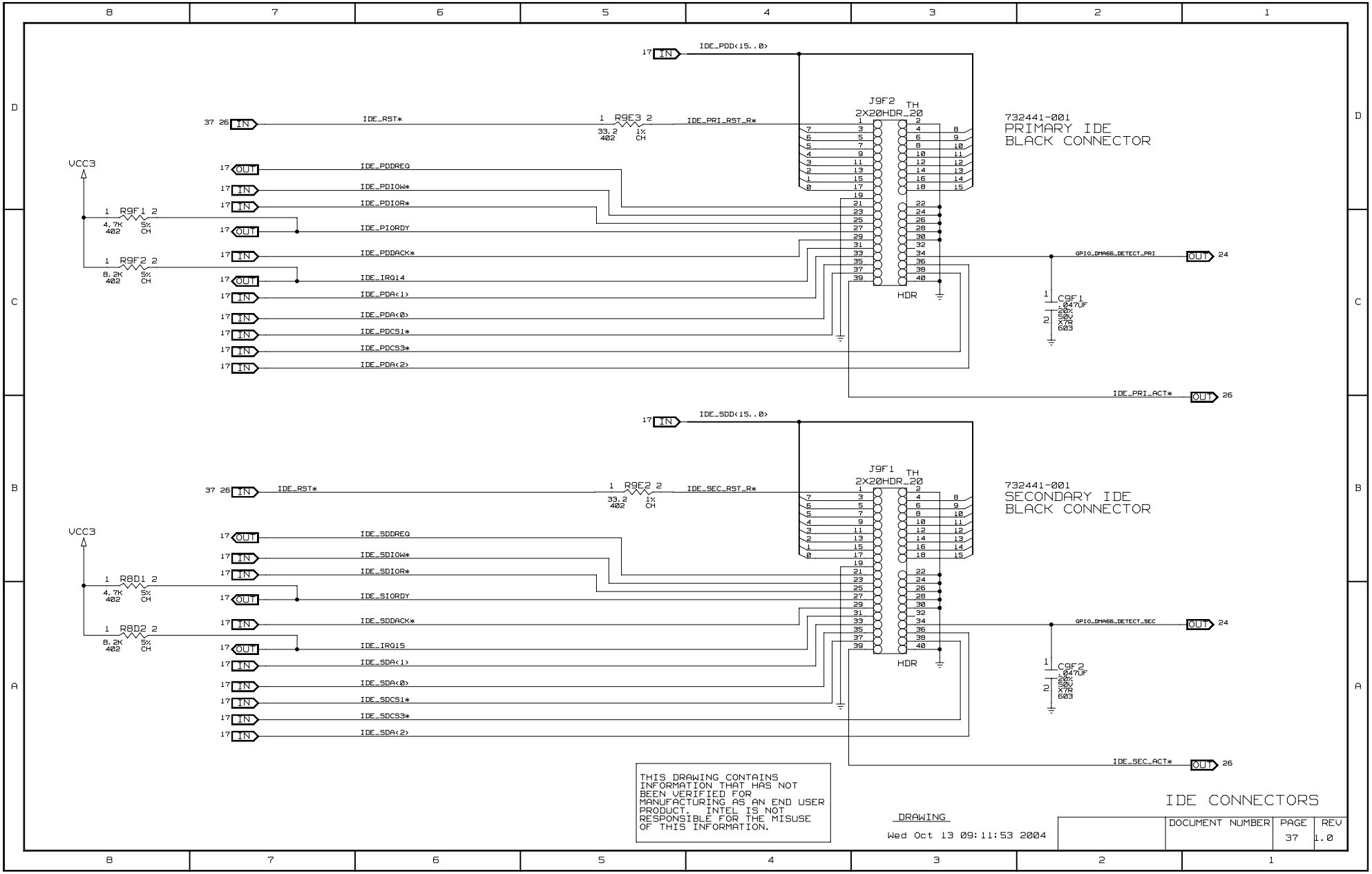
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

DRAWING

Wed Oct 13 09:11:53 2004

SDRAM TERMINATION

	DOCUMENT NUMBER	PAGE	REV
		36	1.0


IDE_PDD<15..0>
J9F2
TH
2X20HDR_20
732441-001
PRIMARY IDE
BLACK CONNECTOR
IDE_RST*
R9E3
33.2
402
1%
CH
IDE_PRI_RST_R*
VCC3
R9F1
4.7K
402
5%
CH
R9F2
8.2K
402
5%
CH
IDE_PDDREQ
IDE_PDIOW*
IDE_PDIOR*
IDE_PIORDY
IDE_PDDACK*
IDE_IRQ14
IDE_PDA<1>
IDE_PDA<0>
IDE_PDCS1*
IDE_PDCS3*
IDE_PDA<2>
GPIO_DMA66_DETECT_PRI
C9F1
.047UF
20%
50V
X7R
603
HDR
IDE_PRI_ACT*
IDE_SDD<15..0>
J9F1
TH
2X20HDR_20
732441-001
SECONDARY IDE
BLACK CONNECTOR
IDE_RST*
R9E2
33.2
402
1%
CH
IDE_SEC_RST_R*
VCC3
R8D1
4.7K
402
5%
CH
R8D2
8.2K
402
5%
CH
IDE_SDDREQ
IDE_SDIOW*
IDE_SDIOR*
IDE_SIORDY
IDE_SDDACK*
IDE_IRQ15
IDE_SDA<1>
IDE_SDA<0>
IDE_SDCS1*
IDE_SDCS3*
IDE_SDA<2>
GPIO_DMA66_DETECT_SEC
C9F2
.047UF
20%
50V
X7R
603
HDR
IDE_SEC_ACT*
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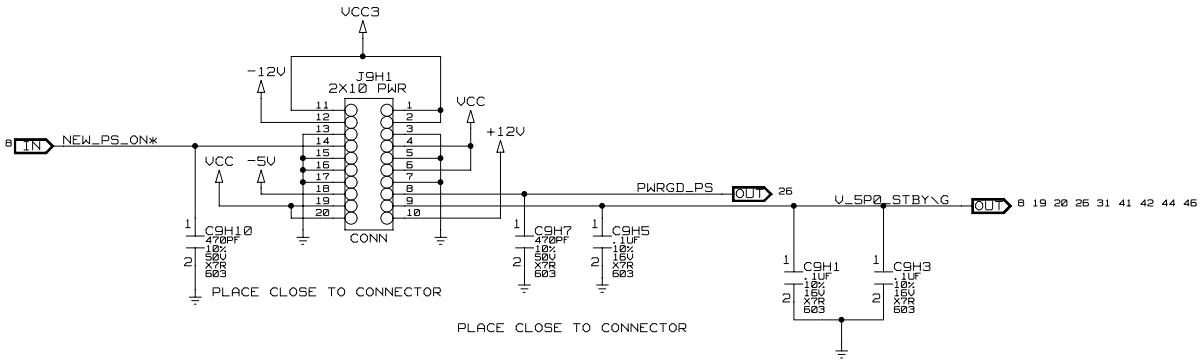
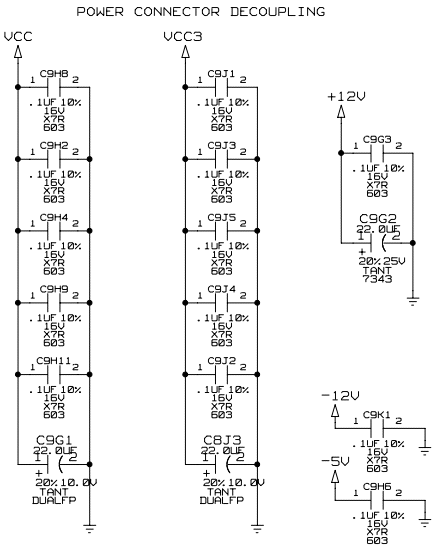
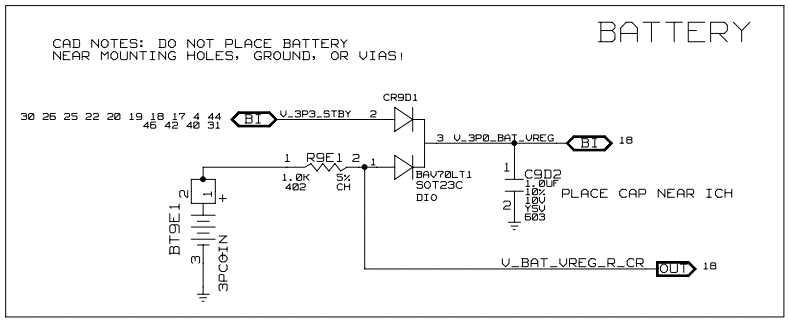
DRAWING
Wed Oct 13 09:11:53 2004
IDE CONNECTORS
DOCUMENT NUMBER
PAGE
37
REV
1.0







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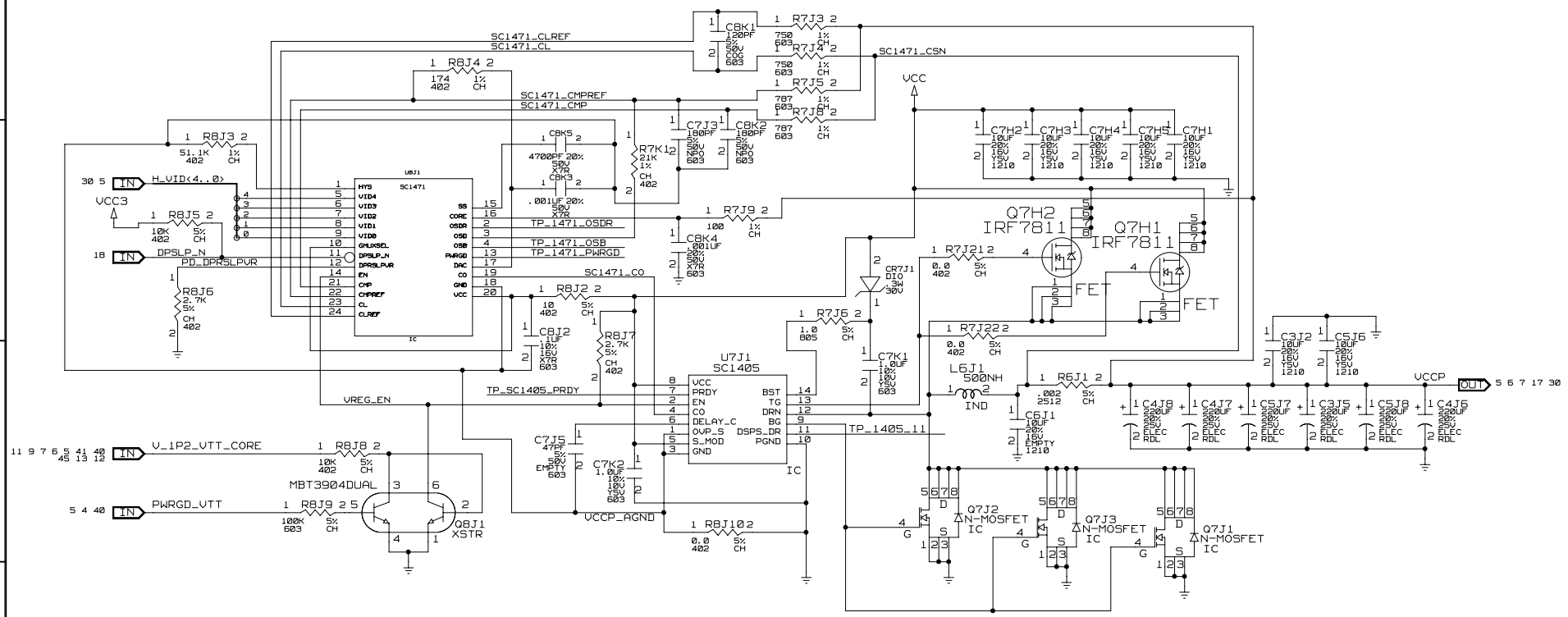
Wed Oct 13 09:11:54 2004

POWER CONN. BATT

	DOCUMENT NUMBER	PAGE	REV
		38	1.0



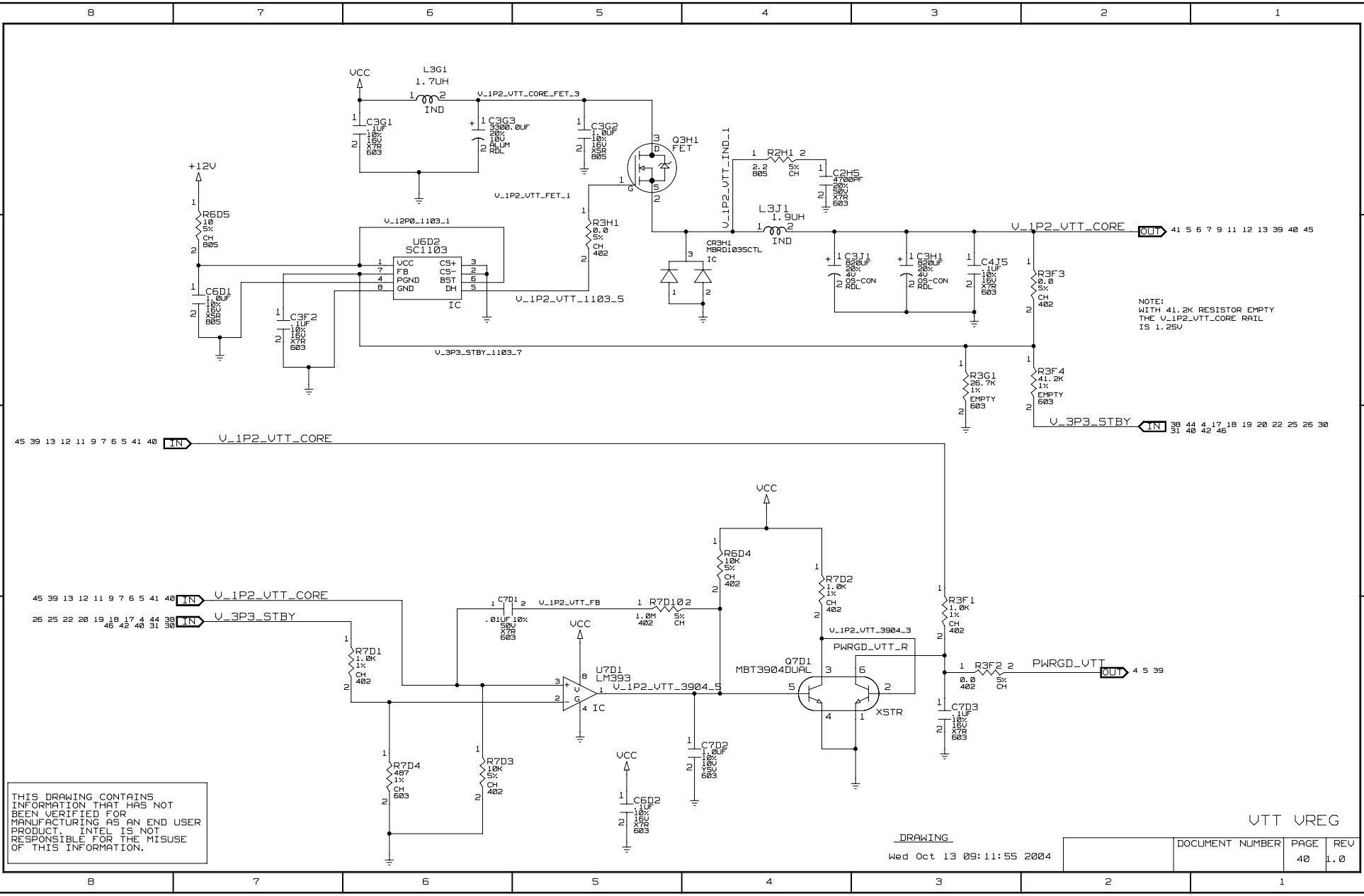
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

DRAWING

Wed Oct 13 09:11:54 2004

CPU VREG

DOCUMENT NUMBER	PAGE	REV
	39	1.0

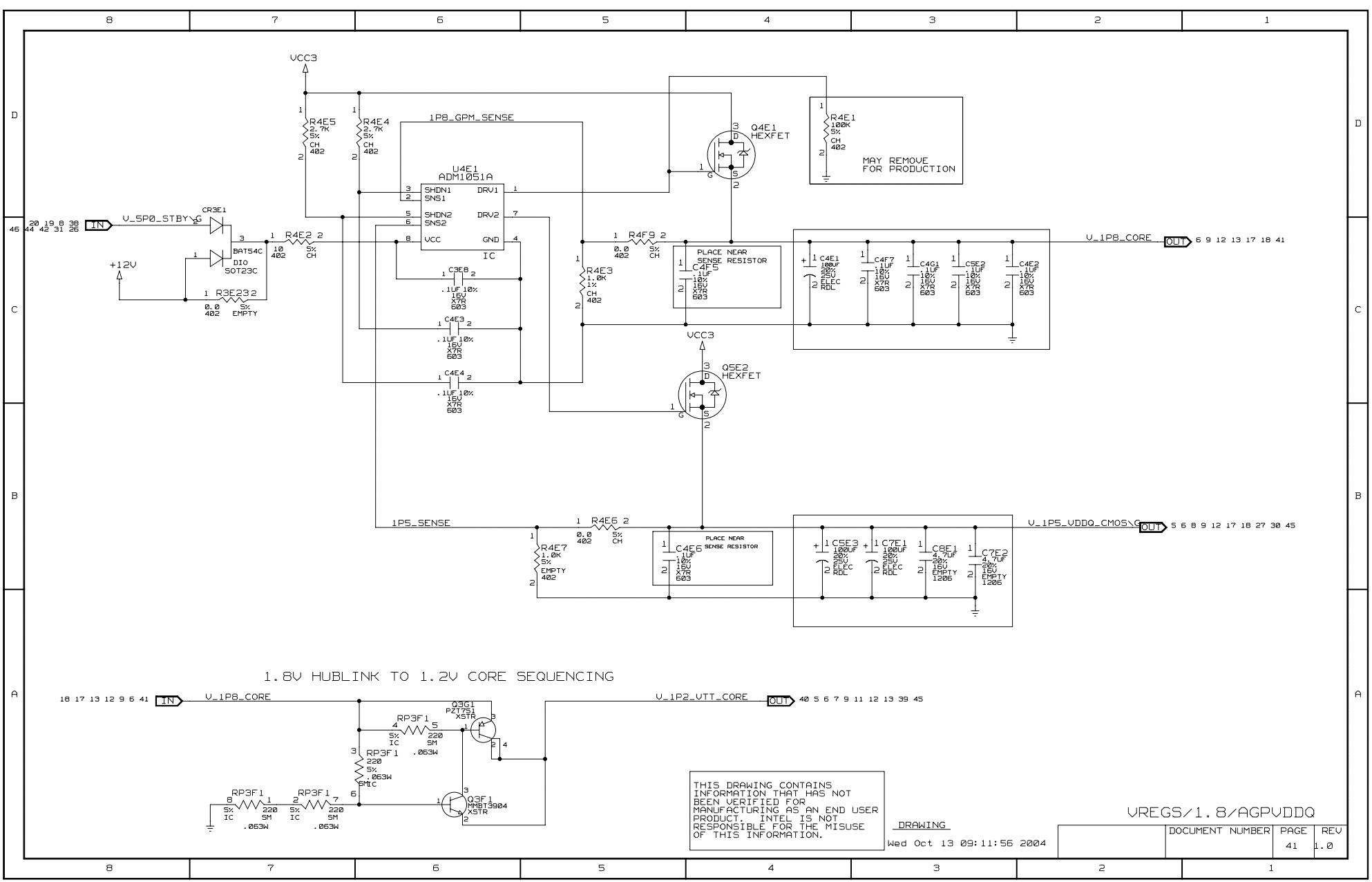


VTT VREG

DRAWING

Wed Oct 13 09:11:55 2004

DOCUMENT NUMBER	PAGE	REV
	40	1.0



1.8V HUBLINK TO 1.2V CORE SEQUENCING

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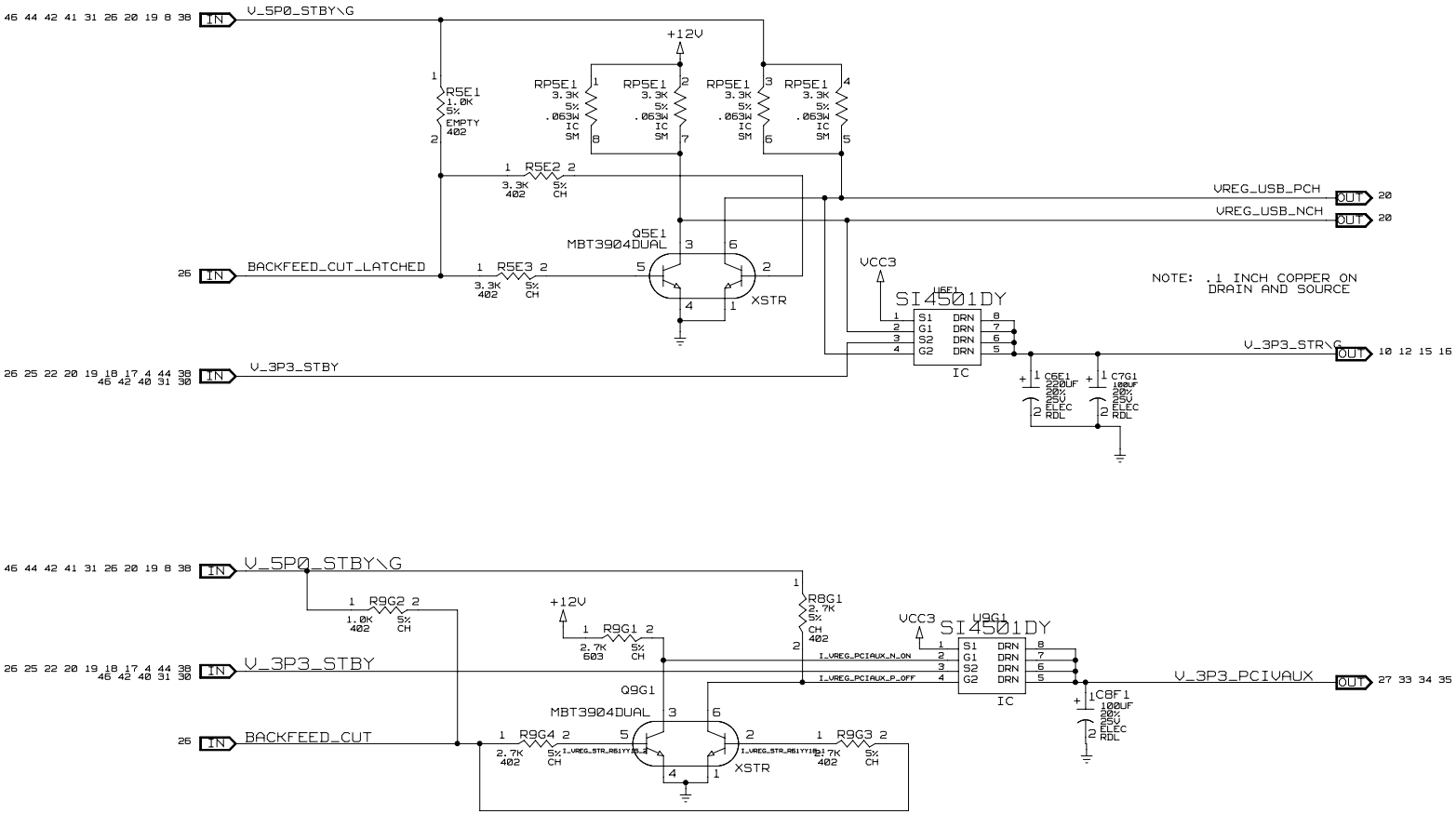
Wed Oct 13 09:11:55 2004

VREGS/1.8/AGPVDDQ

DOCUMENT NUMBER	PAGE	REV
	41	1.0



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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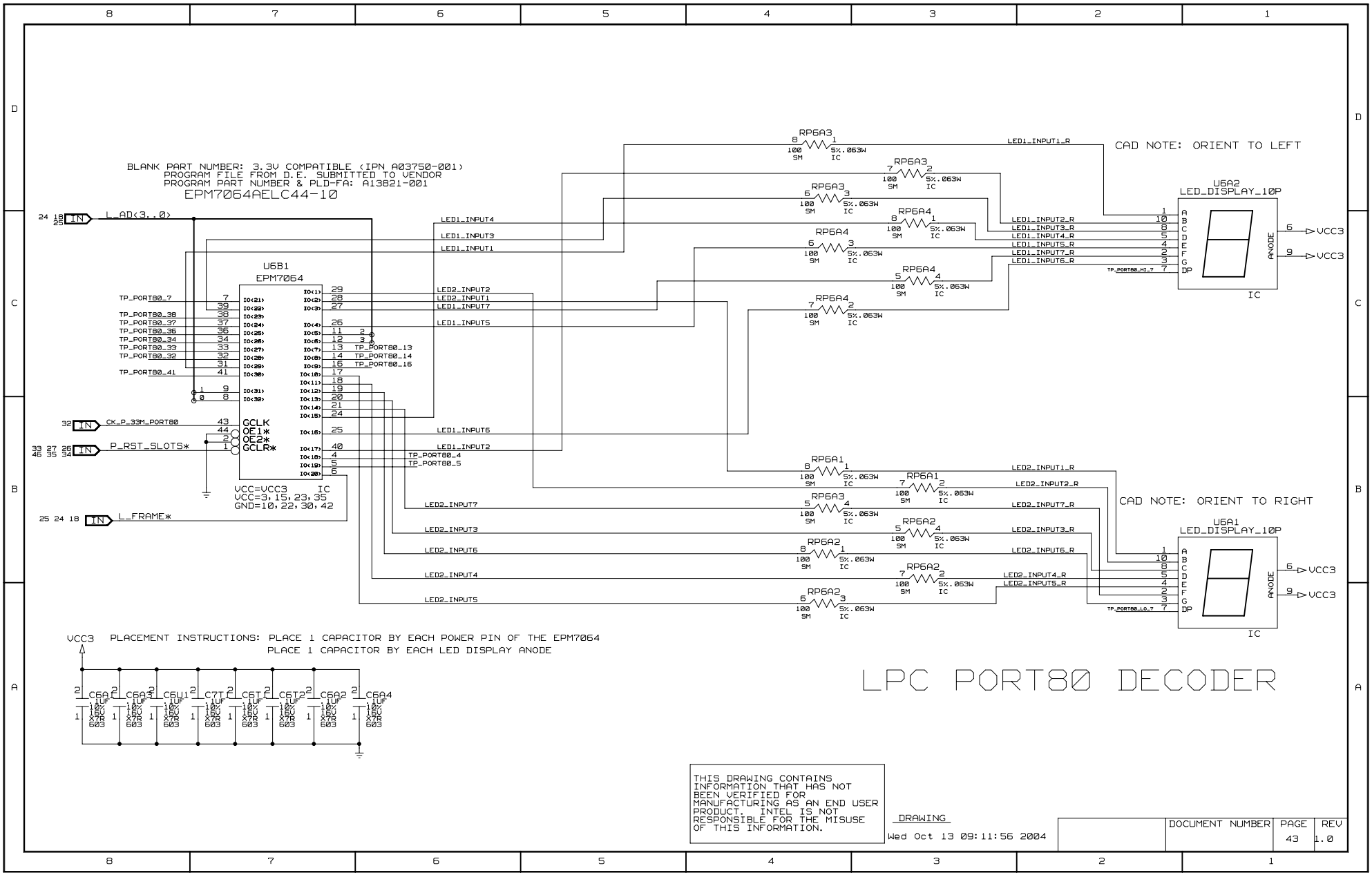
Wed Oct 13 09:11:55 2004

3.3V STR/PCIAUX

	DOCUMENT NUMBER	PAGE	REV
		42	1.0



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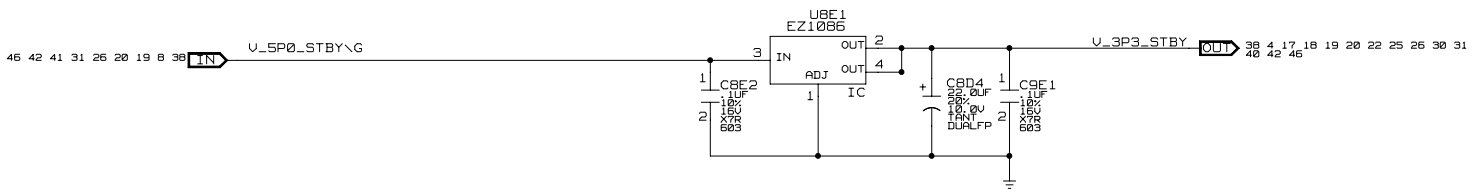
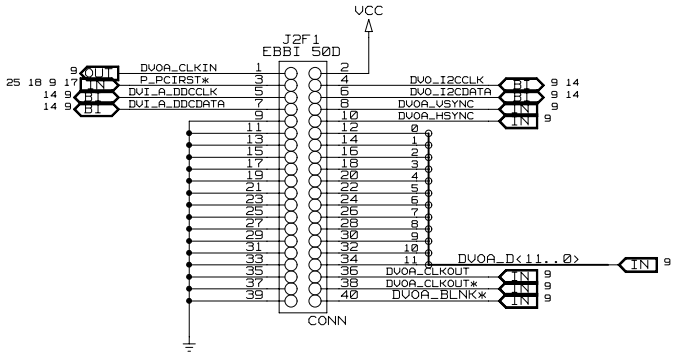
DRAWING

Wed Oct 13 09:11:56 2004

DOCUMENT NUMBER	PAGE	REV
	43	1.0

3.3V STANDBY





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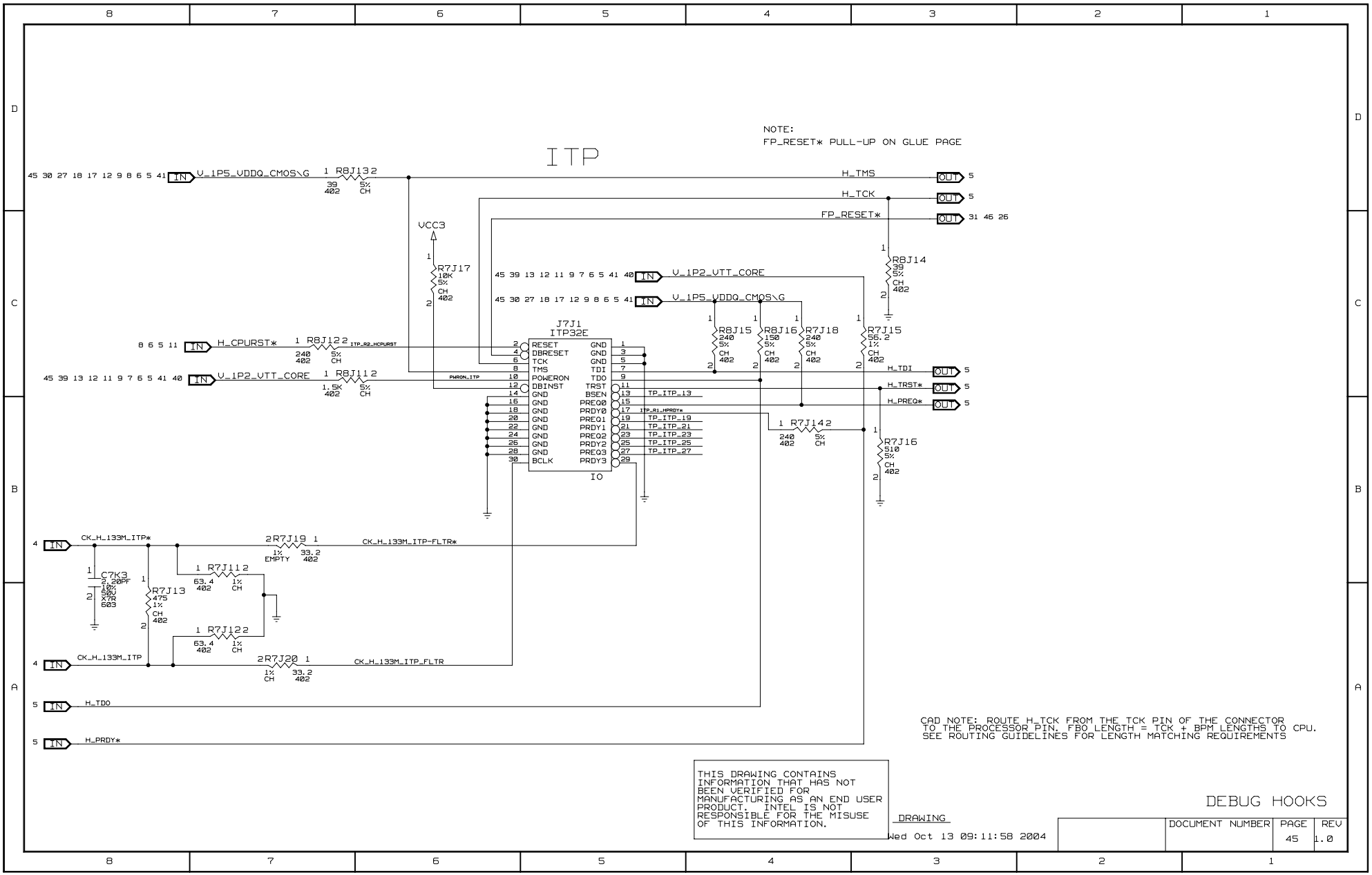
Wed Oct 13 09:11:55 2004

3.3VSB REGULATOR
DVOA INTERFACE

	DOCUMENT NUMBER	PAGE	REV
		44	1.0


ITP
NOTE:
FP_RESET* PULL-UP ON GLUE PAGE
V_1P5_VDDQ_CMOS\G
R8J132
39 5% 402
H_TMS
H_TCK
FP_RESET*
VCC3
R7J17 10K 5% CH 402
V_1P2_VTT_CORE
R8J14 39 5% CH 402
R8J15 240 5% CH 402
R8J16 150 5% CH 402
R7J18 240 5% CH 402
R7J15 56.2 1% CH 402
J7J1
ITP32E
H_CPURST*
R8J122 240 5% CH
ITP_R2_HCPURST
PWRON_ITP
R8J112 1.5K 5% CH
H_TDI
H_TRST*
H_PREQ*
R7J142 240 5% CH
R7J16 510 5% CH 402
IO
RESET DBRESET TCK TMS POWERON DBINST GND BCLK
TRST BSEN PREQ0 PRDY0 PREQ1 PRDY1 PREQ2 PRDY2 PREQ3 PRDY3
TP_ITP_13 TP_ITP_19 TP_ITP_21 TP_ITP_23 TP_ITP_25 TP_ITP_27
ITP_R1_HPRDY*
CK_H_133M_ITP*
R7J19 1% EMPTY 33.2 402
CK_H_133M_ITP-FLTR*
C7K3 2.20PF 10% 50V X7R 603
R7J13 475 1% CH 402
R7J112 63.4 1% CH 402
R7J122 63.4 1% CH 402
CK_H_133M_ITP
R7J20 1% CH 33.2 402
CK_H_133M_ITP_FLTR
H_TDO
H_PRDY*
CAD NOTE: ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN. FBO LENGTH = TCK + BPM LENGTHS TO CPU. SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS
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Wed Oct 13 09:11:58 2004
DEBUG HOOKS
DOCUMENT NUMBER
PAGE 45
REV 1.0

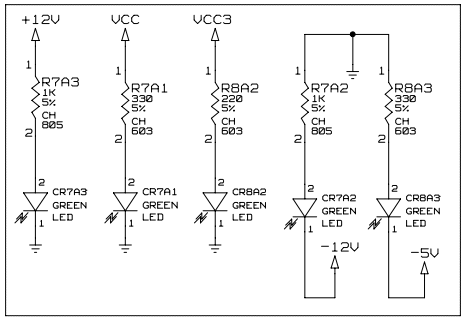
DEBUG LEDS AND SWITCHES

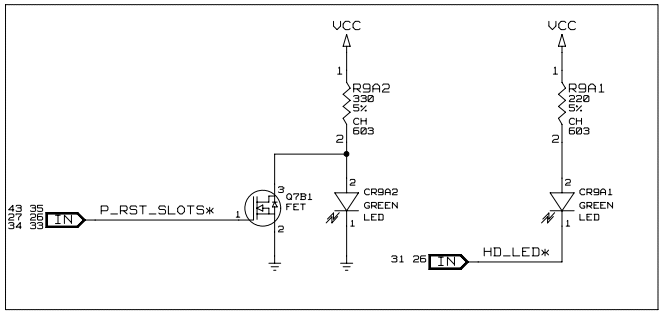
MOUNTING HOLES FOR UATX

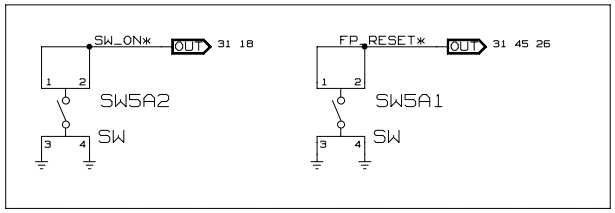
MH9J1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH9A1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH1A1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH1E1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH2J1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH9E1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH1C1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH7E1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8
MH7A1 MTG_HOLE — NC9 — EMPTY — GND=1,2,3,4,5,6,7,8

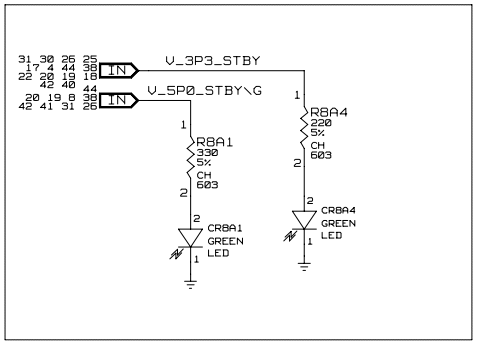
SPARES

RP8C1 10K SM 5% .063W IC
RP6A1 100 SM 5% .063W IC
RP6A1 100 SM 5% .063W IC
RP9C2 330 SM 5% .063W IC
U7D1 LM393 — TP_LM393_7 — IC
CP2E2 10PF SM — 10% 50V EMPTY









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DRAWING
Wed Oct 13 09:11:58 2004

MOUNTING HOLES/DEBUG

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*** Signal Cross-Reference for the entire design ***

A20GATE	25C1> 18D4<
ADD_CLKOUT	27D6> 9A2<
ADD_ID<7..0>	27B3> 9A7<
APICD0_L	18D4<> 19D7<>
APICD1_L	18D4<> 19D7<>
AUD_CD_IN_GND	29D1> 28B7<
AUD_CD_IN_L	29D1> 28B7<
AUD_CD_IN_R	29D1> 28B7<
AUD_LINEOUT_L	28B3> 29A8<
AUD_LINEOUT_R	28B3> 29B8<
AUD_LINE_IN_L	29A1> 28B7<
AUD_LINE_IN_R	29A1> 28B7<
AUD_LINK_BITCLK	28B2<> 18A6<
AUD_LINK_RST*	18A6> 28B7<
AUD_LINK_SDI0	28B2> 18A6<
AUD_LINK_SDO	18A6> 24C2> 28C7<
AUD_LINK_SYNC	18A6> 28B7<
AUD_MIC_IN_1	29B1> 28B7<
AUD_PHONE_IN	29D5> 28B7<
AUD_PHONE_OUT	28B3> 29D8<
AUD_SPDIF_OUT	28B2> 29C8<
AUD_VREF_OUT	28B3> 29B6<
BACKFEED_CUT	26B3> 42A7<
BACKFEED_CUT_LATCHED	26B3> 42C7<
CK_14M_ICH_SIO	4D2> 18C6< 25B6<
CK_32K_SUSCLK	18C4> 25B6<
CK_33M_CPU_APIC	4C2> 6C8<
CK_33M_CPU_APIC_2P0V	6C5> 5C5<
CK_33M_ICH_APIC	4D2> 19C8<
CK_48M_GMCH_DOT	4A2> 9D3<
CK_66M_GBINCLK	4B2> 13A8<
CK_66M_GBOUTCLK	13B1> 4B2<
CK_G_66M_AGP	4A2> 27A8<
CK_HL_66M_ICH	4B2> 18B5<
CK_H_133M_CPU	4A6> 6A8<
CK_H_133M_CPU*	4A6> 6A8<
CK_H_133M_CPU_FLTR	6A4> 5A5<
CK_H_133M_CPU_FLTR*	6A4> 5A5<
CK_H_133M_GMCH	4A6> 11A7<
CK_H_133M_GMCH*	4A6> 11A7<
CK_H_133M_ITP	4A6> 45A8<
CK_H_133M_ITP*	4A6> 45B8<
CK_ICH_APIC	19D5> 18D4<
CK_LPCIO_33M	4D2> 18D2<
CK_LPC_33M_SIO	4C2> 25C6<
CK_P_33M_82551	4B2> 32B8<
CK_P_33M_FWH	4C2> 24C7<
CK_P_33M_ICH	4C2> 17A8<
CK_P_33M_PORT80	32A3> 43B8<
CK_P_33M_SLT0	4B2> 33C3<
CK_P_33M_SLT1	4C2> 34C2<
CK_P_33M_SLT2	4C2> 35C2<
CK_USB_48M_ICH	4A2> 18A2<
DPSLP_N	18C4> 39C8<
DVI_A_DDCCLK	9D3> 44B6<> 14D4<
DVI_A_DDCDATA	9D3> 44B6<> 14D4<
DVI_BC_DDCCLK	9A7<> 27D3<>
DVI_BC_DDCDATA	9A7<> 27D3<>
DVOA_BLNK*	9C5> 44B4<
DVOA_CLKIN	44C6> 9C5<
DVOA_CLKOUT	9C5> 44B4<
DVOA_CLKOUT*	9C5> 44B4<
DVOA_D<11..0>	9D5> 44B3<
DVOA_HSYNC	9C5> 44B4<
DVOA_VSYNC	9C5> 44B4<
DVOB_BLNK*	9A7> 27D6>
DVOB_CLKOUT	9A7> 27B8<
DVOB_CLKOUT*	9A7> 27B8<

DVOB_D<0>	9B4>
DVOB_D<11..0>	27B8<
DVOB_D<1>	9B4>
DVOB_D<2>	9B4>
DVOB_D<3>	9B4>
DVOB_D<4>	9A4>
DVOB_D<5>	9B4>
DVOB_D<6>	9A4>
DVOB_D<7>	9A7>
DVOB_D<8>	9A4>
DVOB_D<9>	9A4>
DVOB_D<10>	9A4>
DVOB_D<11>	9A4>
DVOB_FLD	9A2> 27C8<
DVOB_HSYNC	9B4> 27B8<
DVOB_VSYNC	9B4> 27B8<
DVOC_BLNK*	9A4> 27C8<
DVOC_CLKOUT	9A7> 27B8<
DVOC_CLKOUT*	9A7> 27B8<
DVOC_D<0>	9A4>
DVOC_D<11..0>	27C8<
DVOC_D<1>	9A4>
DVOC_D<2>	9A4>
DVOC_D<3>	9A4>
DVOC_D<4>	9A4>
DVOC_D<5>	9A7>
DVOC_D<6>	9A4>
DVOC_D<7>	9A4>
DVOC_D<8>	9A4>
DVOC_D<9>	9A4>
DVOC_D<10>	9A4>
DVOC_D<11>	9A4>
DVOC_FLD	9A4> 27D8<
DVOC_HSYNC	9A4> 27C8<
DVOC_VSYNC	9A4> 27C8<
DVO_BC_I2CCLK	9A7<> 27D3<>
DVO_BC_I2CDATA	9A7<> 27D3<>
DVO_BC_INTR*	27D6> 9A2<
DVO_I2CCLK	9D3> 44B4<> 14C4<
DVO_I2CDATA	9D3> 44B4<> 14D4<
EE_CLK	18A5> 23A8<
EE_CS	18A5> 23A8<
EE_DIN	23A6> 18A5<
EE_DOUT	18A7> 23A8<
FAN1_CTRL	30D6> 30B8<
FAN1_TACH	30B1> 30C3<
FAN2_CTRL	30D3> 30B8<
FAN2_TACH	30B2> 30C3<
FAN3_CTRL	30C3> 30A8<
FAN3_TACH	30A1> 30C3<
FP_GPIO<7..0>	18A2<> 31A5<>
FP_RESET*	31D2> 45C3> 46C4> 26D7<
GLUE4_DDCSCL_3V	9D3<> 26B8<>
GLUE4_DDCSCL_5V	9B3<> 26B8<>
GLUE4_DDCSDA_3V	9D3<> 26B8<>
GLUE4_DDCSDA_5V	9B3<> 26B8<>
GLUE_FP_RST_R*	26D5> 26B6<
GPIO_DMA66_DETECT_PRI	37C1> 24B7<
GPIO_DMA66_DETECT_SEC	37A1> 24B7<
GPIO_GRN_BLNK_HDR	26A3> 31C7<
GPIO_LAN_ENABLE	18C8> 22A5<
GPIO_SIO_PME_OUT*	25C6> 18D6<
GPIO_YLW_BLNK_HDR	26A3> 31C7<
G_AD15	9A4<> 27C8<>
G_CBE2*	9A7<> 27B8<>
G_GNT*	9B7> 27C3<
G_PAR	9A7<> 27C3<>
G_PIPE*	27C3> 9A7<
G_RBF*	27C3> 9A7<
G_REQ*	27C3> 9A7<

G_SBSTB	27B8> 9B7<
G_SBSTB*	27B8> 9B7<
G_ST0	9B7> 27D8<
G_ST1	9B7> 27D8<
G_ST2	9B7> 27D8<
G_STOP*	9A7<> 27C3<>
G_WBF*	27C3> 9A7<
HD_LED*	26A3> 31D2> 46C2<
HL<10..0>	13C7<> 18B5<>
HL_PSTB	13C6<> 18B5<>
HL_PSTB*	13C6<> 18B5<>
H_A#<31..3>	5D6<> 11D5<>
H_A20M*	18D4> 5B4<
H_ADS*	5D2<> 11B6<>
H_APICD0	5C5<> 6C8<> 19D5<>
H_APICD1	5C5<> 6C8<> 19D5<>
H_BNR*	5C5<> 11B6<>
H_BPRI*	11B6<> 5C5<
H_BREQ0*	6A1> 5C5<
H_BSEL0	5D5> 4C6< 6B8<
H_BSEL1	5D5> 4C6< 6B8<
H_CPURST*	11B6> 5D5< 6B1< 8B7< 45C8<
H_D#<63..0>	5D8<> 11D5<>
H_DBSY*	5C2<> 11B6<>
H_DEFER*	11B6<> 5D2<
H_DRDY*	5C2<> 11B6<>
H_FERR*	5B4> 6C8> 18D4<
H_FLUSH*	6D8> 5D5<
H_HIT*	5D2<> 11B6<>
H_HITM*	5D2<> 11B6<>
H_IGNNE*	18D4> 5B4<
H_INIT*	18D4> 5D5< 6D8< 24A7<
H_INTR	18D4> 5D5<
H_LOCK*	5C5> 11B6<>
H_NMI	18D4> 5D5<
H_PRDY*	5A4> 45A8<
H_PREQ*	45B3> 5A4<
H_PWRGD	18D4> 5D5< 6D8<
H_REQ#<4..0>	5C5<> 11A6<>
H_RS#<2..0>	5C2<> 11B6<>
H_SLP*	18D4> 5B5<
H_SMI*	18D4> 5D5<
H_STPCLK*	18D3> 5A4<
H_TCK	45D3> 5A4<
H_TDI	45C3> 5A4<
H_TDO	5A4> 45A8<
H_TESTHI<0>	6B1> 5B5<
H_TESTHI<1>	6B1> 5B5<
H_TESTLO<0>	6A1> 5A5<
H_TESTLO<1>	6A1> 5B5<
H_TMS	45D3> 5A4<
H_TRDY*	5D2<> 11A6<>
H_TRST*	45C3> 5A4<
H_VID<4..0>	5A2> 30C6< 39C8<
ICH_FP_RST_R*	26D5> 18C6<
ICH_RSMRST*	26B3> 18C4<
IDE_IRQ14	37C7> 17C5<
IDE_IRQ15	37A7> 17C5<
IDE_PDA<0>	17C7> 37C7<
IDE_PDA<1>	17C7> 37C7<
IDE_PDA<2>	17C7> 37C7<
IDE_PDCS1*	17C7> 37C7<
IDE_PDCS3*	17C7> 37C7<
IDE_PDD<15..0>	17D8<> 37D5<
IDE_PDDACK*	17C7> 37C7<
IDE_PDDREQ	37D7> 17C7<
IDE_PDIOR*	17C7> 37D7<
IDE_PDIOW*	17C7> 37D7<
IDE_PIORDY	37C7> 17C7<
IDE_PRI_ACT*	37C1> 26B6<

IDE_RST*	26B3> 37B7< 37D7<
IDE_SDA<0>	17C5> 37A7<
IDE_SDA<1>	17C5> 37A7<
IDE_SDA<2>	17C5> 37A7<
IDE_SDCS1*	17C5> 37A7<
IDE_SDCS3*	17C5> 37A7<
IDE_SDD<15..0>	17D5<> 37B5<
IDE_SDDACK*	17C5> 37A7<
IDE_SDDREQ	37B7> 17C5<
IDE_SDIOR*	17C5> 37B7<
IDE_SDIOW*	17C5> 37B7<
IDE_SEC_ACT*	37A1> 26B6<
IDE_SIORDY	37A7> 17C5<
KBRST*	25C1> 18D4<
LAN_ACT_LED*	22B3> 23C8<
LAN_CLK	22D1> 18A5<
LAN_LILED*	22B3> 23C5>
LAN_RDN	23C5> 22C6<
LAN_RDP	23C5> 22C6<
LAN_RST	18A5> 22C6<
LAN_RXD0	22C3> 18A5<
LAN_RXD1	22C3> 18A5<
LAN_RXD2	22C3> 18A5<
LAN_SPEEDLED*	22B3> 23C5>
LAN_TDN	22C3> 23D8<
LAN_TDP	22C3> 23D8<
LAN_TXD0	18A5> 22C6<
LAN_TXD1	18A5> 22C6<
LAN_TXD2	18A5> 22C6<
L_AD<3..0>	18C4<> 18D2<> 24D4<> 25C6<> 43C8<
L_DRQ*	25C6> 18C4<
L_DRQ1*	18D2> 18C4<
L_FRAME*	18C4> 18D2< 24C7< 25C6< 43B8<
NCHCTRLP_R	6B1> 5A5<
NEW_PS_ON*	8B2> 38D8<
PLL1_C	5B2> 6C4<
PLL2_C	6C1> 5B2<
PS2_PULLUPS	20A2> 31C5<
PS_ON*	26B3> 8A7<
PWRGD_3V	26B3> 18C4< 20D7< 24D8<
PWRGD_PS	38D5> 26A8<
PWRGD_VTT	40A2> 4A8< 5C2< 39B8<
P_AD<31..0>	17B6<> 32D8<> 33A3<> 33A8<> 33C8<> 34A2<> 34A7<> 34C7<> 35A2<> 35A7<> 35C8<>
P_C/BE*<3..0>	17A4<> 32B8<> 33B3<> 33B8<> 34B2<> 34B7<> 35B2<> 35B7<>
P_DEVSEL*	17A8<> 32B8<> 33B3<> 34B2<> 35B2<> 19C3<
P_FRAME*	17A8<> 32B8<> 33C8<> 34B7<> 35B7<> 19C3<
P_GNT*<4..0>	32B8<>
P_GNT*<5..0>	17A8> 33C8< 34C7< 35C7<
P_INTA*	27A8<> 33D8> 34D2> 35D7> 17B8< 19B3<
P_INTB*	27A8<> 33D3> 34D7> 35C2> 17B8< 19B3<
P_INTC*	33D8> 34C2> 35D7> 17B8< 19B3<
P_INTD*	33D3> 34D7> 35D2> 17B8< 19B3<
P_INTE*	17B8< 19B3<
P_INTF*	17B8< 19B3<
P_INTG*	32B8> 17B8< 19B3<
P_INTH*	17B8< 19B3<
P_IRDY*	17A8<> 32B8<> 33B3<> 34B2<> 35B2<> 19C3<
P_PAR	17A8<> 32B8<> 33B8<> 34B7<> 35B7<>
P_PCIREQA*	17A8< 19B3<
P_PCIRST*	17A8> 9D3< 18D3< 25C6< 44B6<

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P_PERR*          17A8<> 32B8<> 33B3> 34B2> 35B2>
                 19C3<
P_PLOCK*         17A8<> 33B3<> 34B2<> 35B2<> 19C3<
P_PME*           19A1> 27A8<> 33C8> 34C7> 35C7>
                 17A8<
P_REQ*<4..0>     32B8<>
P_REQ*<5..0>     17B8< 19C3< 33C3< 34C2< 35C2<
P_RST*           26B3> 24C7< 32B8<
P_RST_SLOTS*     26B3> 27A8< 33C8< 34C7< 35C7<
                 43B8< 46C4<
P_SERR*          32B8<> 33B3> 34B2> 35B2> 17A8<
                 19C3<
P_STOP*          17A8<> 32B8<> 33B8<> 34B7<> 35B7<>
                 19C3<
P_TRDY*          17A8<> 32B8<> 33B8<> 34B7<> 35B7<>
                 19C3<
RTTCTRL          6A1> 5B2<
SER_IRQ          18D2<> 18D4<> 25C6<>
SIO_KBCLOCK      31B6<> 25C1<
SIO_KBDATA       31B6<> 25C1<
SIO_MSCLOCK      31B6<> 25C1<
SIO_MSDATA       31B6<> 25C1<
SLEWCTRL         6A1> 5A5<
SLP_S3*          18C6> 26B6<
SLP_S5*          18C6> 26B6<
SMB_CLK          15B7<> 18C8<> 19B7<> 26C8<> 30D6<>
                 31A5<> 32B4<> 4C6<
SMB_CLK_ISO      19B7<> 26C8<> 33B8<> 34B7<> 35B7<>

SMB_DATA         4C6<> 15B7<> 18C8<> 19B7<> 26C8<>
                 30D6<> 31A8<> 32B4<>
SMB_DATA_ISO     19B7<> 26B8<> 33B8<> 34B7<> 35B7<>

SM_BA<1..0>      10C8> 15B7< 16B8<
SM_CAS*          10C8> 15B7< 16D8<
SM_CKE0          10C5> 15B7<
SM_CKE1          10C5> 15B7<
SM_CKE2          10C5> 16D8<
SM_CLK0          10B6> 15C7<
SM_CLK1          10B6> 15B7<
SM_CLK2          10B6> 16D8<
SM_CS0*          10C5> 15B7<
SM_CS1*          10C5> 15B7<
SM_CS2*          10C5> 16D8<
SM_DQM<7..0>     10B6> 15B7< 16B8<
SM_MA<12..0>     10D8> 15B7< 16B8<
SM_MD<63..0>     10D2<> 36D7<> 36D8<>
SM_MD_RAM<63..0>  16D8<> 36D3<> 36D4<>
SM_MD_SKT<63..0>  15B7<> 36D3<> 36D4<> 36D7<>
                 36D8<>
SM_RAS*          10C8> 15B7< 16D8<
SM_WE*           10C8> 15B7< 16D8<
SW_ON*           31D5> 46C5> 18C6<
THERMALDN        5A5> 30D6<
THERMALDP        30D6> 5A5<
THERMTRIP_R*     5C2> 8C7<
USB_FP_OC*       21A1> 20C7<
USB_ICH_OC0_1*   20C2> 18B2<
USB_ICH_OC2_3*   20A2> 18B2<
USB_ICH_OC4_5*   20B2> 18B2<
USB_ICH_P0       18B2<> 21D8<>
USB_ICH_P0*      18B2<> 21D8<>
USB_ICH_P1       18B2<> 21C8<>
USB_ICH_P1*      18B2<> 21D8<>
USB_ICH_P2       18B2<> 21C8<>
USB_ICH_P2*      18B2<> 21C8<>
USB_ICH_P3       18B2<> 21B8<>
USB_ICH_P3*      18B2<> 21B8<>
USB_ICH_P4       18B2<> 21B8<>
USB_ICH_P4*      18B2<> 21B8<>
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USB_ICH_P5       18B2<> 21A8<>
USB_ICH_P5*      18B2<> 21A8<>
VCCP             39B1> 5D2< 6C4< 7D5< 17B4< 30D3<
VREG_PS2         20A2> 31C3<
VREG_USB1        20B2> 21D3<
VREG_USB2        20B2> 21B3<
VREG_USB3        20A2> 21C3<
VREG_USB_NCH     42C2> 20B7<
VREG_USB_PCH     42C2> 20B7<
V_0P8_GTLREF     11B8> 5A3<
V_1P0_CMOS_REF   6D1> 5B5<
V_1P2_VTT_CORE   40C2> 41A4> 5D2< 6C4< 7D8< 9B5<
                 9B8< 11C8< 11D3< 12A8< 13D7< 39B8<
                 40B8< 40B8< 45C5< 45C8<
V_1P5_STBY       19A4> 17B4<
V_1P5_VDDQ_CMOS  41B2> 5B4< 6D4< 6D8< 8D7< 9A2<
                 9B8< 9C4< 12A8< 17B4< 17C4< 18D8<
                 27D8< 30D3< 45C5< 45D8<
V_1P8_CORE       41C1> 6D8< 9B8< 9D8< 12A8< 12D7<
                 13B8< 17B4< 18B7< 41A8<
V_3P0_BAT_VREG   38A5<> 18C3< 18C4<
V_3P3_PCIVAUX    42A2> 27A8< 33C8< 34C7< 35C7<
V_3P3_STBY       38A7<> 44D3> 4A8< 17C4< 18D8<
                 19A3< 20C7< 22A4< 25D5< 25D6< 26D7<
                 30D3< 31D8< 40A8< 40B2< 42A7< 42C7<
                 46C3<
V_3P3_STR        42C2> 10A5< 10B3< 10C2< 12D8<
                 15A7< 15D7< 16A7<
V_5P0_STBY       38D4> 8B7< 19A7< 20B7< 26C7< 31C8<
                 41C8< 42B7< 42D7< 44D8< 46C3<
V_BAT_VREG_R_CR  38A5> 18C1<
V_REF5V          26C3> 17B4<
V_REF5V_SUS      26C3> 17B4<
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*** Part Cross-Reference for the entire design ***

BT9E1 BATT_HLDR_2PIN 38
C1D1 MCE_CAPN 29
C1D2 MCE_CAPN 29
C1D3 MCE_CAPN 29
C1D4 MCE_CAPN 29
C1D5 CAPN 28
C1D6 MCE_CAPN 29
C1D7 MCE_CAPN 28
C1D8 MCE_CAPN 28
C1D9 MCE_CAPN 28
C1D10 CAPN 28
C1E1 CAPN 29
C1E2 CAPN 29
C1E3 CAPN 22
C1E4 MCE_CAPN 22
C1E5 CAPN 29
C1E6 CAPN 23
C1F1 CAPN 23
C1F2 MCE_CAPN 23
C1F3 MCE_CAPN 29
C1F4 MCE_CAPN 29
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